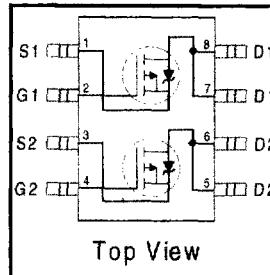


PRELIMINARY

IRF7314

HEXFET® Power MOSFET

- Generation V Technology
- Ultra Low On-Resistance
- Dual P-Channel MOSFET
- Surface Mount
- Fully Avalanche Rated



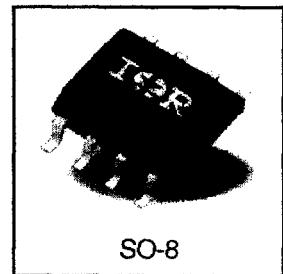
$V_{DSS} = -20V$

$R_{DS(on)} = 0.058\Omega$

Description

Fifth Generation HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design for which HEXFET Power MOSFETs are well known, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The SO-8 has been modified through a customized leadframe for enhanced thermal characteristics and multiple-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infrared, or wave soldering techniques.



Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	-20	V
V_{GS}	Gate-to-Source Voltage	± 8.0	
$I_D @ T_A = 25^\circ C$	Continuous Drain Current ⑤	-5.3	
$I_D @ T_A = 70^\circ C$	Continuous Drain Current ⑤	-4.3	A
I_{DM}	Pulsed Drain Current ①	-21	
I_S	Continuous Source Current (diode conduction)	-2.5	
$P_D @ T_A = 25^\circ C$	Max. Power Dissipation ⑥	2.0	W
$P_D @ T_A = 70^\circ C$	Max. Power Dissipation ⑥	1.3	
E_{AS}	Single Pulse Avalanche Energy ②	150	mJ
I_{AR}	Avalanche Current	-2.9	A
E_{AR}	Repetitive Avalanche Energy	0.20	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance Ratings

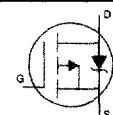
	Parameter	Limit	Units
$R_{θJA}$	Maximum Junction-to-Ambient ⑤	62.5	°C/W

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	-20	—	—	V
$\Delta V_{(\text{BR})\text{DSS}/\Delta T_J}$	Breakdown Voltage Temp. Coefficient	—	0.031	—	V/ $^\circ\text{C}$
$R_{\text{DS}(\text{on})}$	Static Drain-to-Source On-Resistance	—	0.049	0.058	Ω
		—	0.082	0.098	
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	-0.70	—	—	V
g_{fs}	Forward Transconductance	—	5.9	—	S
I_{DS}	Drain-to-Source Leakage Current	—	—	-1.0	μA
		—	—	-25	
I_{GS}	Gate-to-Source Forward Leakage	—	—	100	nA
	Gate-to-Source Reverse Leakage	—	—	-100	
Q_g	Total Gate Charge	—	19	29	nC
Q_{gs}	Gate-to-Source Charge	—	4.0	6.1	
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	7.7	12	
$t_{\text{d}(\text{on})}$	Turn-On Delay Time	—	15	22	ns
t_r	Rise Time	—	40	60	
$t_{\text{d}(\text{off})}$	Turn-Off Delay Time	—	42	63	
t_f	Fall Time	—	49	73	
C_{iss}	Input Capacitance	—	780	—	pF
C_{oss}	Output Capacitance	—	470	—	
C_{rss}	Reverse Transfer Capacitance	—	240	—	

Source-Drain Ratings and Characteristics

Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-2.5	A
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-21	
V_{SD}	Diode Forward Voltage	—	-0.78	-1.0	V
t_{rr}	Reverse Recovery Time	—	47	71	ns
Q_{rr}	Reverse Recovery Charge	—	49	73	nC



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (see figure 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 35\text{mH}$, $R_G = 25\Omega$, $I_{AS} = -2.9\text{A}$.
- ③ $I_{SD} \leq -2.9\text{A}$, $dI/dt \leq -77\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(\text{BR})\text{DSS}}$, $T_J \leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ Surface mounted on FR-4 board, $t \leq 10$ sec.

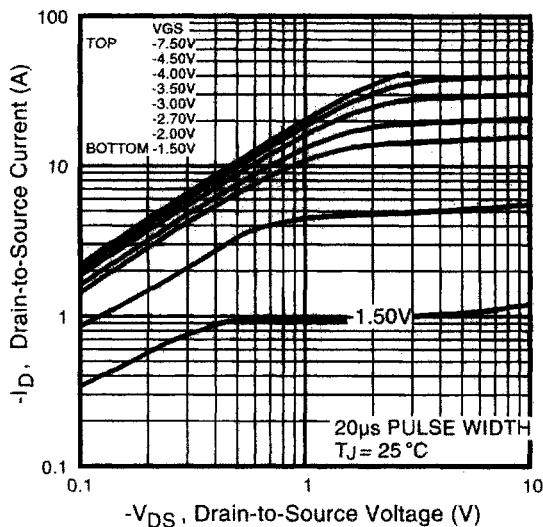


Fig 1. Typical Output Characteristics

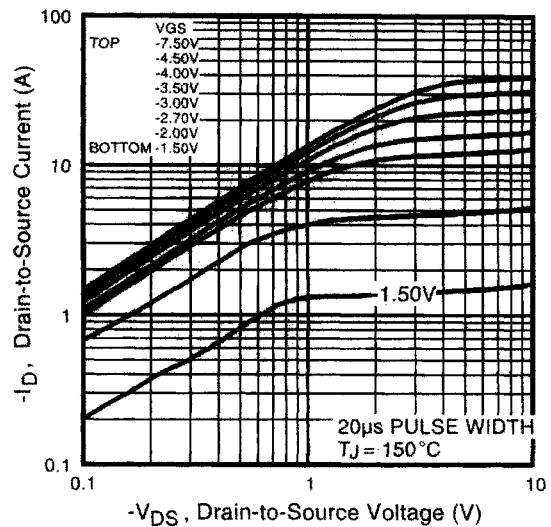


Fig 2. Typical Output Characteristics

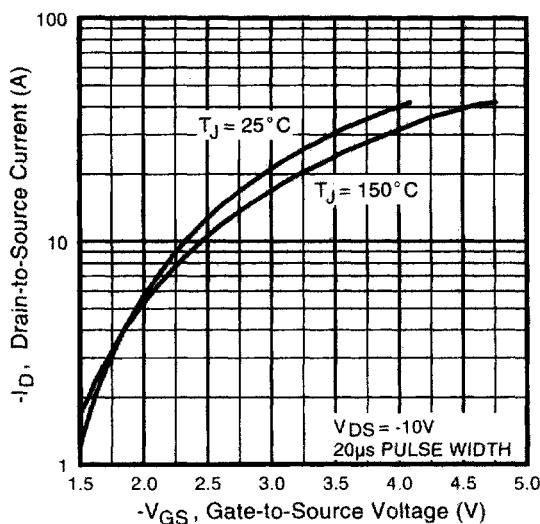


Fig 3. Typical Transfer Characteristics

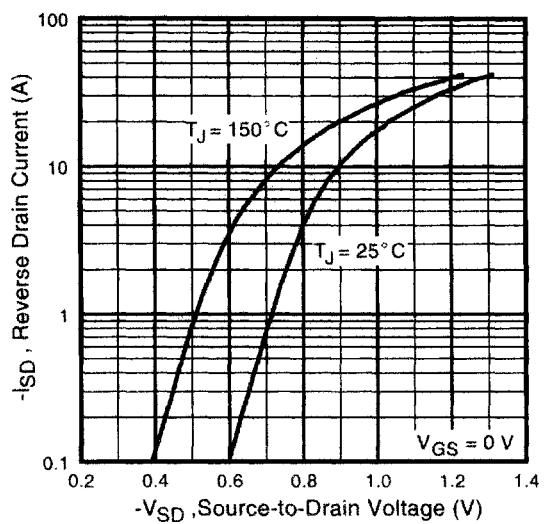


Fig 4. Typical Source-Drain Diode Forward Voltage

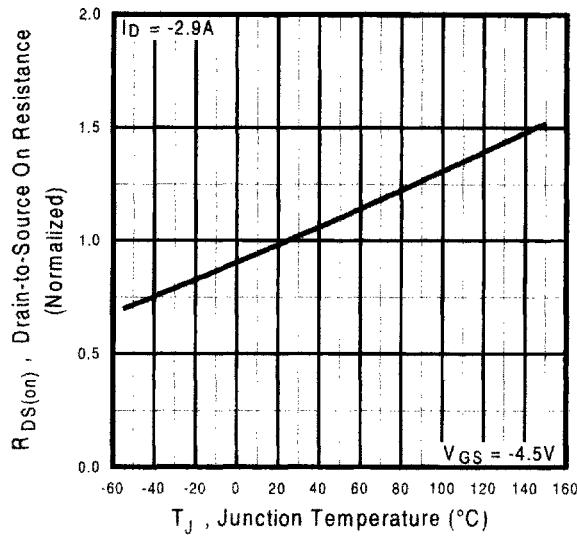


Fig 5. Normalized On-Resistance Vs. Temperature

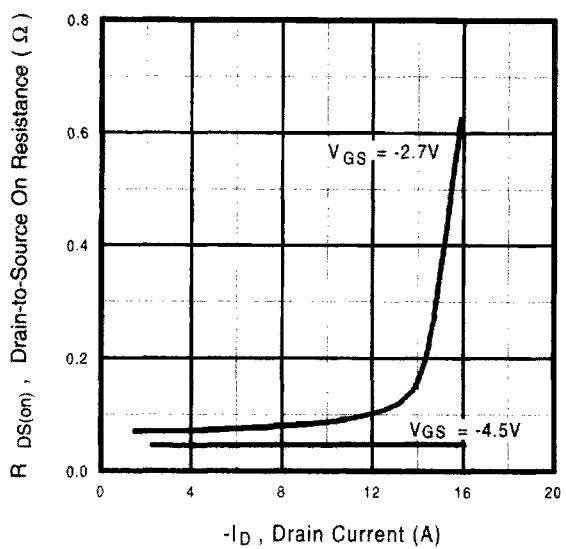


Fig 6. Typical On-Resistance Vs. Drain Current

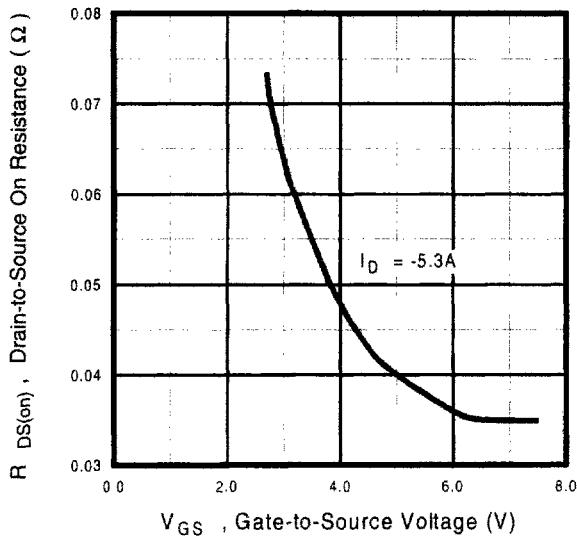


Fig 7. Typical On-Resistance Vs. Gate Voltage

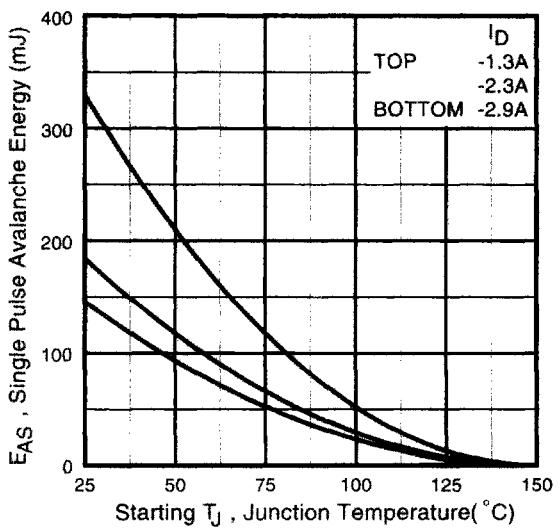


Fig 8. Maximum Avalanche Energy Vs. Drain Current

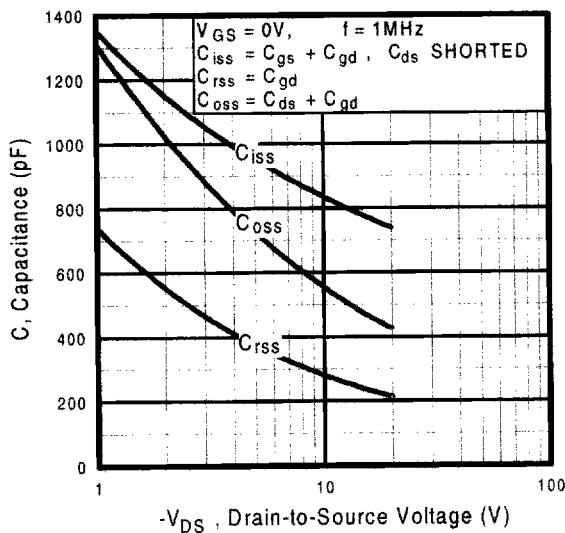


Fig 9. Typical Capacitance Vs.
Drain-to-Source Voltage

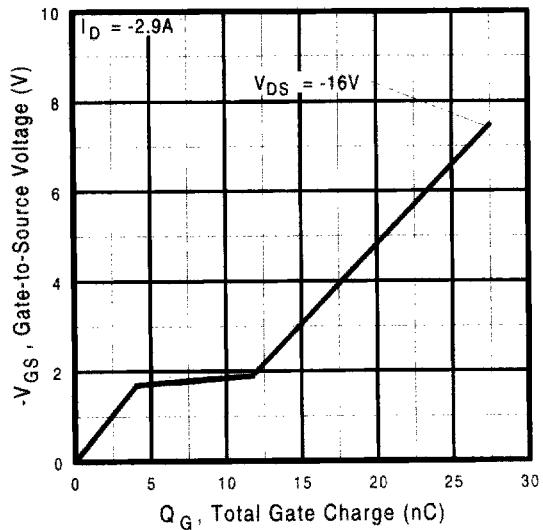


Fig 10. Typical Gate Charge Vs.
Gate-to-Source Voltage

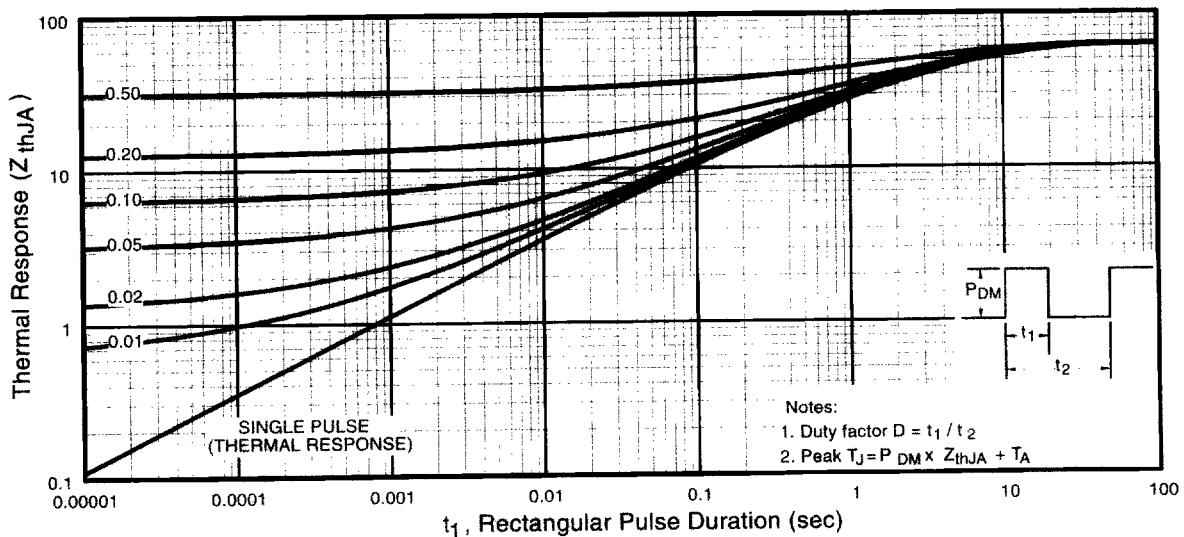


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

Mechanical drawings, Appendix A

Part marking information, Appendix B

Test Circuit diagrams, Appendix C