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April 1st, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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HD74HC273 Octal D-type Flip-Flops (with Clear)

> REJ03D0604-0300 Rev.3.00 Mar 25, 2009

Description

This device contains 8 master-slave flip-flops with a common clock and common clear. Data on the D input having the specified setup and hold times is transferred to the Q output on the low to high transition of the clock input. The clear input when low, sets all outputs to a low state.

Features

- High Speed Operation: t_{pd} (Clock to Q) = 18 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2 \text{ to } 6 \text{ V}$
- Low Input Current: 1 µA max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max (Ta = 25°C)
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC273P	DILP-20 pin	PRDP0020AC-B (DP-20NEV)	Р	—
HD74HC273FPEL	SOP-20 pin (JEITA)	PRSP0020DD-B (FP-20DAV)	FP	EL (2,000 pcs/reel)
HD74HC273RPEL	SOP-20 pin (JEDEC)	PRSP0020DC-A (FP-20DBV)	RP	EL (1,000 pcs/reel)
HD74HC273TELL	TSSOP-20 pin	PTSP0020JB-A (TTP-20DAV)	Т	ELL (2,000 pcs/reel)

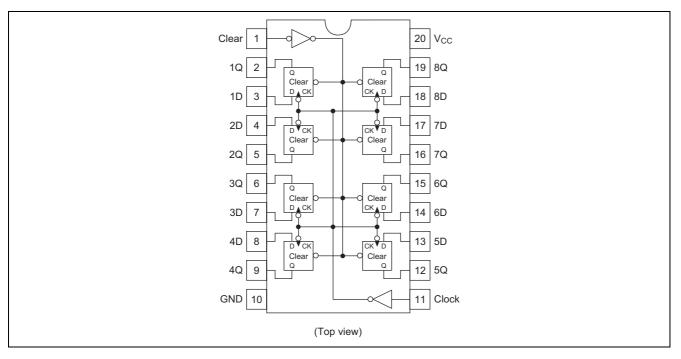
Note: Please consult the sales office for the above package availability.

Function Table

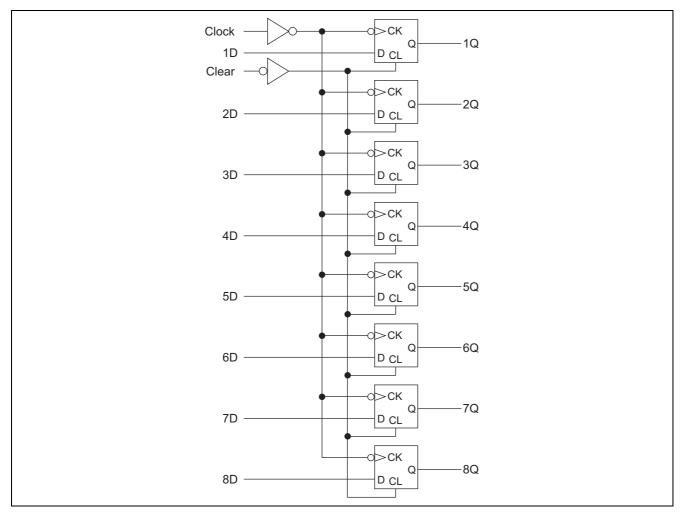
	Output		
Clear	Clock	D	Q
L	X	Х	L
Н		Н	н
Н		L	L
Н	L	Х	No change
Н		Х	No change

Note 1. H: high level, L: low level, X: irrelevant

Pin Arrangement



Logic Diagram



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Absolute Maximum Ratings

ltem	Symbol	Ratings	Unit
Supply voltage range	V _{CC}	-0.5 to 7.0	V
Input / Output voltage	V _{IN} , V _{OUT}	–0.5 to V _{CC} +0.5	V
Input / Output diode current	I _{IK} , I _{OK}	±20	mA
Output current	lo	±25	mA
V _{CC} , GND current	I _{CC} or I _{GND}	±50	mA
Power dissipation	PT	500	mW
Storage temperature	Tstg	-65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions	
Supply voltage	V _{CC}	2 to 6	V		
Input / Output voltage	V _{IN} , V _{OUT}	0 to V _{CC}	V		
Operating temperature	Та	-40 to 85	°C		
Input rise / fall time ^{*1}		0 to 1000		V _{CC} = 2.0 V	
	t _r , t _f	0 to 500 ns V _{CC} =		$V_{CC} = 4.5 V$	
		0 to 400		$V_{CC} = 6.0 V$	

Notes: 1. This item guarantees maximum limit when one input switches. Waveform: Refer to test circuit of switching characteristics.

Electrical Ch	aracteristics
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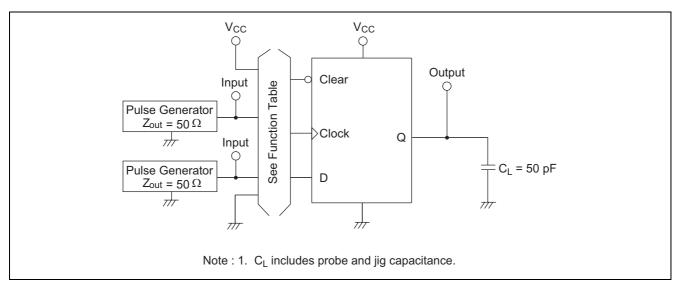
Itom	Symbol		Т	a = 25°	С	Ta = -40	to+85°C	Unit	Test Conditions				
ltem	Symbol	V _{cc} (V)	Min	Тур	Max	Min	Max	Unit					
	V _{IH}	2.0	1.5			1.5	—						
		4.5	3.15	_	_	3.15	—	V					
Input voltage		6.0	4.2	_	_	4.2	—						
Input voltage		2.0	_	_	0.5	—	0.5						
	VIL	4.5	_	_	1.35	—	1.35	V					
		6.0			1.8		1.8						
		2.0	1.9	2.0		1.9	—						
	V _{он}	4.5	4.4	4.5	_	4.4	—	V	$Vin = V_{IH} \text{ or } V_{IL}$ $I_{OH} =$	I _{OH} = −20 μA			
		6.0	5.9	6.0	_	5.9	—						
		4.5	4.18	_	_	4.13	—			I _{OH} = -4 mA			
Output voltage		6.0	5.68	_	_	5.63	—			I _{OH} = -5.2 mA			
Oulput vollage		2.0	_	0.0	0.1	—	0.1						
		4.5	_	0.0	0.1	—	0.1		Vin = V _{IH} or V _{IL} $I_{OL} = 4 \text{ mA}$	I _{OL} = 20 μA			
	V _{OL}	6.0	_	0.0	0.1	—	0.1	V					
		4.5	_	_	0.26	—	0.33			$I_{OL} = 4 \text{ mA}$			
		6.0	_	_	0.26	—	0.33			I _{OL} = 5.2 mA			
Off-state output current	I _{OZ}	6.0			±0.5	_	±5.0	μΑ	$Vin = V_{IH} \text{ or } V_{IL},$ $Vout = V_{CC} \text{ or } G$	ND			
Input current	lin	6.0	_	_	±0.1	—	±1.0	μA	$Vin = V_{CC} \text{ or } GN$	D			
Quiescent supply current	I _{CC}	6.0	_	_	4.0	—	40	μA	$Vin = V_{CC} \text{ or } GN$	D, lout = 0 µA			

Switching Characteristics

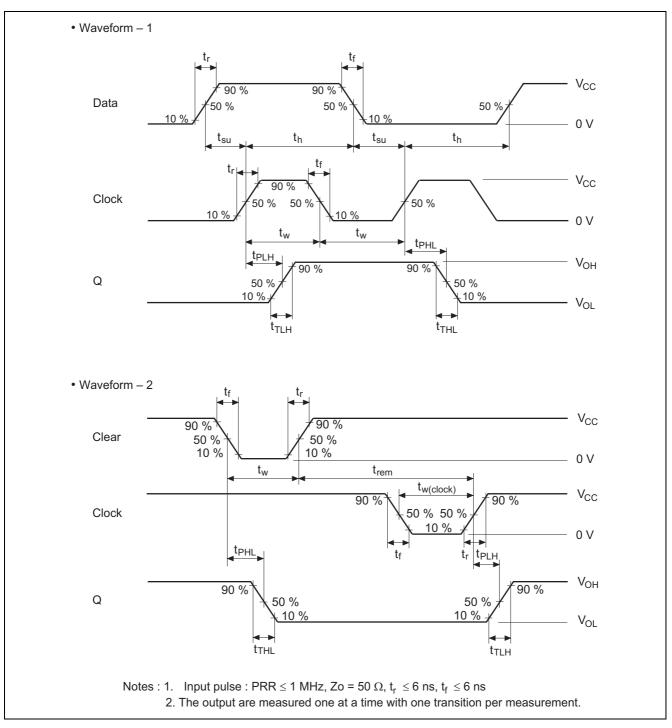
 $(C_L = 50 \text{ pF}, \text{ Input } t_r = t_f = 6 \text{ ns})$

Item	Symbol	V 00	Ta = 25°C			Ta = -40 to +85°C		l la it	Test Osnelitions
		V _{cc} (V)	Min	Тур	Max	Min	Max	Unit	Test Conditions
		2.0		—	6	—	5	MHz	
Maximum clock	f _{max}	4.5	_	_	30	—	24		
frequency		6.0	_	—	35	—	28		
		2.0	_	_	145	—	180		
	t _{PHL}	4.5	_	18	29	—	36	ns	Clock to Q
		6.0	_	_	25	—	31		
		2.0	_	_	145	—	180		
Propagation delay time	t _{PLH}	4.5	_	18	29	—	36	ns	
		6.0	_	_	25	—	31		
		2.0		—	145	—	180	ns	
	t _{PHL}	4.5		15	29	—	36		Clear to Q
		6.0		—	25	—	31		
		2.0	100	—	_	125	—	ns	Data to clock
Setup time	t _{su}	4.5	20	2	—	25	—		
		6.0	17	—	_	21	_		
		2.0	5	—	_	5	_	ns	Clock to data
Hold time	t _h	4.5	5	0	_	5	_		
		6.0	5	—	_	5	—		
		2.0	100	—	_	125	—		Clear to clock
Removal time	t _{rem}	4.5	20	-1	_	25	—	ns	
		6.0	17	—	_	21	—		
		2.0	80	—	_	100	_		Clock, clear
Pulse width	t _w	4.5	16	8	_	20	_	ns	
		6.0	14	—	—	17	—		
	+	2.0		—	75	—	95	ns	
Output rise/fall time	t _{TLH}	4.5		5	15	—	19		
	t _{THL}	6.0		—	13	—	16		
Input capacitance	Cin	—	_	5	10	—	10	рF	

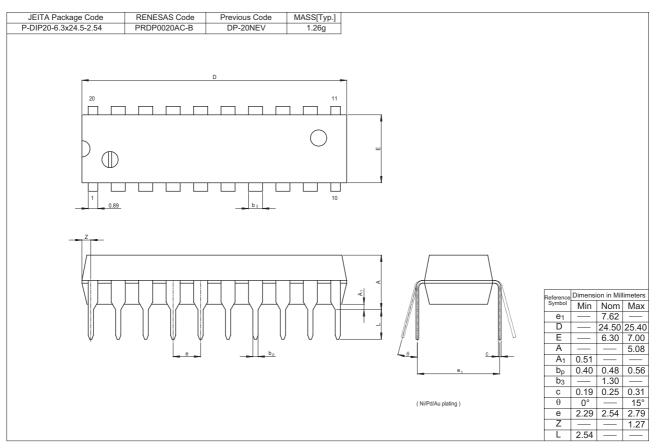
Test Circuit

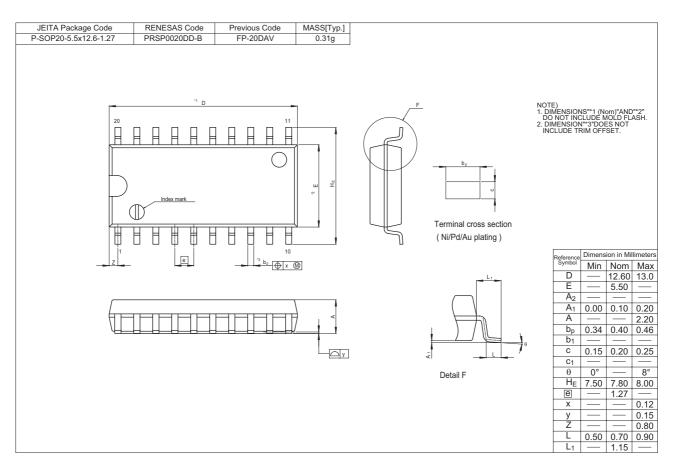


Waveforms



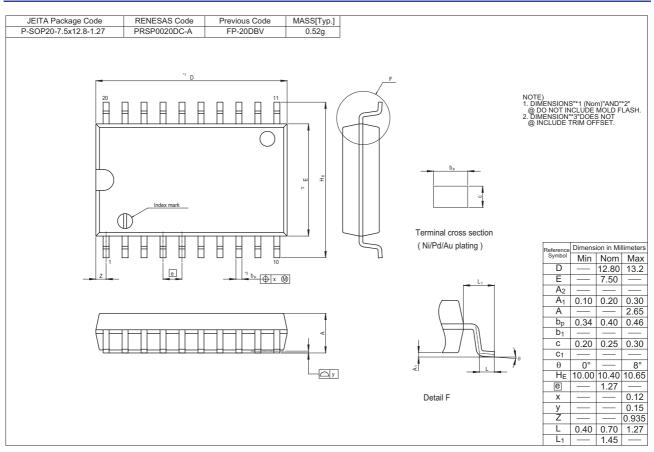
Package Dimensions

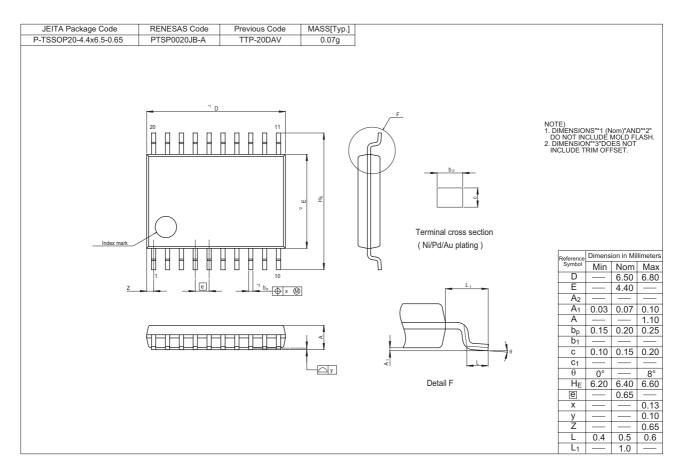




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