Quad 2-input AND gate Rev. 7 — 16 April 2020

**Product data sheet** 

### 1. General description

The 74HC08; 74HCT08 is a quad 2-input AND gate. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

### 2. Features and benefits

- Complies with JEDEC standard JESD7A
- Input levels:
  - For 74HC08: CMOS level
  - For 74HCT08: TTL level
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

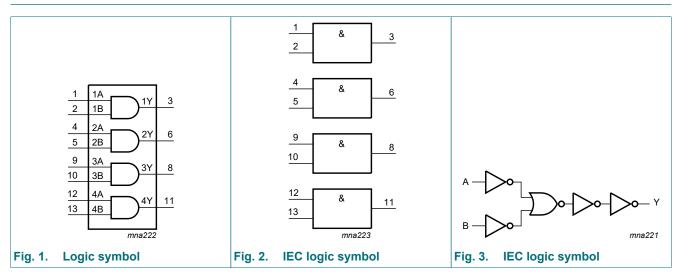
### 3. Ordering information

### Table 1. Ordering information

Type number	Package					
	Temperature range	Name	Description	Version		
74HC08D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads;	SOT108-1		
74HCT08D			body width 3.9 mm			
74HC08DB	-40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads;	SOT337-1		
74HCT08DB			body width 5.3 mm			
74HC08PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads;	SOT402-1		
74HCT08PW			body width 4.4 mm			
74HC08BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced	SOT762-1		
74HCT08BQ			very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm			

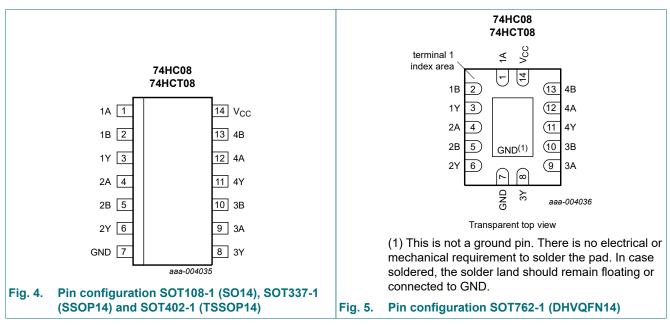
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### 4. Functional diagram



# 5. Pinning information





### 5.2. Pin description

Table 2. Pin description						
Symbol	Pin	Description				
1A, 2A, 3A, 4A	1, 4, 9, 12	data input				
1B, 2B, 3B, 4B	2, 5, 10, 13	data input				
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data output				
GND	7	ground (0 V)				
V <sub>CC</sub>	14	supply voltage				

<sup>74</sup>HC\_HCT08

### 6. Functional description

#### Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input	Output	
nA	nB	nY
L	L	L
L	Н	L
Н	L	L
Н	Н	Н

### 7. Limiting values

#### Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7	V
I <sub>IK</sub>	input clamping current	$V_{\rm I} < -0.5 \text{ V or } V_{\rm I} > V_{\rm CC} + 0.5 \text{ V}$ [1]	-	±20	mA
I <sub>OK</sub>	output clamping current	$V_{\rm O}$ < -0.5 V or $V_{\rm O}$ > $V_{\rm CC}$ + 0.5 V [1]	-	±20	mA
lo	output current	$-0.5 V < V_O < V_{CC} + 0.5 V$	-	±25	mA
I <sub>CC</sub>	supply current		-	50	mA
I <sub>GND</sub>	ground current		-50	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 to +85 °C [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT108-1 (SO14) package: P<sub>tot</sub> derates linearly with 10.1 mW/K above 100 °C.

For SOT337-1 (SSOP14) package: Ptot derates linearly with 7.3 mW/K above 81 °C.

For SOT402-1 (TSSOP14) package: Ptot derates linearly with 7.3 mW/K above 81 °C.

For SOT762-1 (DHVQFN14) package: Ptot derates linearly with 9.6 mW/K above 98 °C.

### 8. Recommended operating conditions

#### Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	ions 74HC08			Unit			
			Min	Тур	Max	Min	Тур	Max	
V <sub>CC</sub>	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
VI	input voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
Vo	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	-	+125	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 2.0 V	-	-	625	-	-	-	ns/V
		V <sub>CC</sub> = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V <sub>CC</sub> = 6.0 V	-	-	83	-	-	-	ns/V

# 9. Static characteristics

### Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol Parameter		Conditions		25 °C			°C to 5 °C	-40 °C to +125 °C		Unit
			Min	Тур	Мах	Min	Max	Min	Max	-
74HC08					-	-				
V <sub>IH</sub>	HIGH-level	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
	input voltage	V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
	V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V	
VIL	LOW-level	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
	input voltage	V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
	V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V	
V <sub>OH</sub> HIGH-level	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>									
	output voltage	I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
	I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V	
	I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V	
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I <sub>O</sub> = -5.2 mA; V <sub>CC</sub> = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V <sub>OL</sub>	LOW-level	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
	output voltage	I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I	input leakage current	$V_{I} = V_{CC}$ or GND; $V_{CC} = 6.0$ V	-	-	±0.1	-	±1	-	±1	μA
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	2.0	-	20	-	40	μA
CI	input capacitance		-	3.5	-	-	-	-	-	pF

### Quad 2-input AND gate

Symbol	Parameter	Conditions		25 °C			°C to 5 °C	-40 °C to +125 °C		Unit
			Min	Тур	Мах	Min	Мах	Min	Max	
74HCT08	}	1				1				_
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V <sub>OH</sub> HIGH-level		$V_{I} = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$								
	output voltage	I <sub>O</sub> = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
OL -	LOW-level	$V_{I} = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$								
	output voltage	I <sub>O</sub> = 20 μA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 5.2 mA	-	0.15	0.26	-	0.33	-	0.4	V
l <sub>l</sub>	input leakage current	$V_{I} = V_{CC}$ or GND; $V_{CC} = 5.5 V$	-	-	±0.1	-	±1	-	±1	μA
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	2.0	-	20	-	40	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}; I_O = 0 \text{ A};$ other inputs at $V_{CC}$ or GND; $V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	60	216	-	270	-	294	μA
CI	input capacitance		-	3.5	-	-	-	-	-	pF

# **10.** Dynamic characteristics

### Table 7. Dynamic characteristics

 $GND = 0 V; C_L = 50 pF;$  for test circuit see Fig. 7.

Symbol	ool Parameter Conditions		25 °C		-40 °C to +85 °C		-40 °C to +125 °C		Unit	
			Min	Тур	Max	Min	Max	Min	Max	
74HC08	-									
t <sub>pd</sub>	propagation	nA, nB to nY; see Fig. 6 [1]								
delay	V <sub>CC</sub> = 2.0 V	-	25	90	-	115	-	135	ns	
	V <sub>CC</sub> = 4.5 V	-	9	18	-	23	-	27	ns	
	V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	7	-	-	-	-	-	ns	
		V <sub>CC</sub> = 6.0 V	-	7	15	-	20	-	23	ns
t <sub>t</sub>	transition time	see <u>Fig. 6</u> [2]								
		V <sub>CC</sub> = 2.0 V	-	19	75	-	95	-	110	ns
		V <sub>CC</sub> = 4.5 V	-	7	15	-	19	-	22	ns
		V <sub>CC</sub> = 6.0 V	-	6	13	-	16	-	19	ns
C <sub>PD</sub>	power dissipation capacitance	per package; [3] $V_I = GND$ to $V_{CC}$	-	10	-	-	-	-	-	pF

74HC\_HCT08

### Quad 2-input AND gate

Symbol	Parameter	Conditions		25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
					Тур	Max	Min	Max	Min	Max	1
74HCT08	5										
t <sub>pd</sub> propagation	nA, nB to nY; see Fig. 6	[1]									
	delay	V <sub>CC</sub> = 4.5 V		-	14	24	-	30	-	36	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF		-	11	-	-	-	-	-	ns
t <sub>t</sub>	transition time	V <sub>CC</sub> = 4.5 V; see <u>Fig. 6</u>	[2]	-	7	15	-	19	-	22	ns
C <sub>PD</sub>	power dissipation capacitance	per package; V <sub>I</sub> = GND to V <sub>CC</sub> - 1.5 V	[3]	-	20	-	-	-	-	-	pF

[1]  $t_{pd}$  is the same as  $t_{PHL}$  and  $t_{PLH}$ .

 $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ): [2] [3]

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$  where:

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

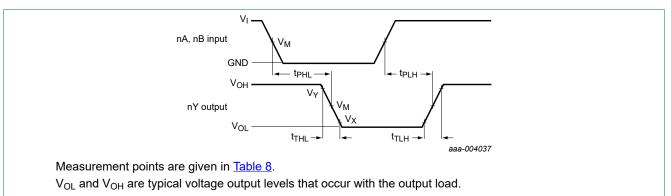
C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

 $\sum (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs.}$ 

### 10.1. Waveforms and test circuit

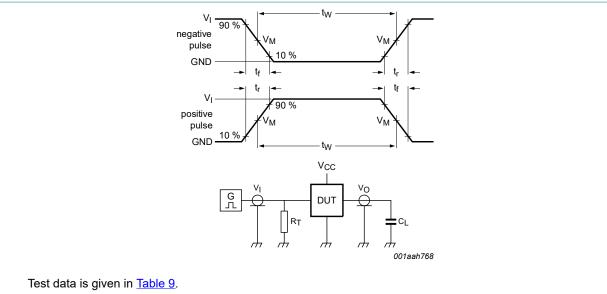


#### Fig. 6. Input to output propagation delays

#### **Table 8. Measurement points**

Туре	Input	Output					
	V <sub>M</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>			
74HC08	0.5V <sub>CC</sub>	0.5V <sub>CC</sub>	0.1V <sub>CC</sub>	0.9V <sub>CC</sub>			
74HCT08	1.3 V	1.3 V	0.1V <sub>CC</sub>	0.9V <sub>CC</sub>			

### **Quad 2-input AND gate**



Definitions test circuit:

 $R_{T}$  = termination resistance should be equal to output impedance  $\mathsf{Z}_{o}$  of the pulse generator.

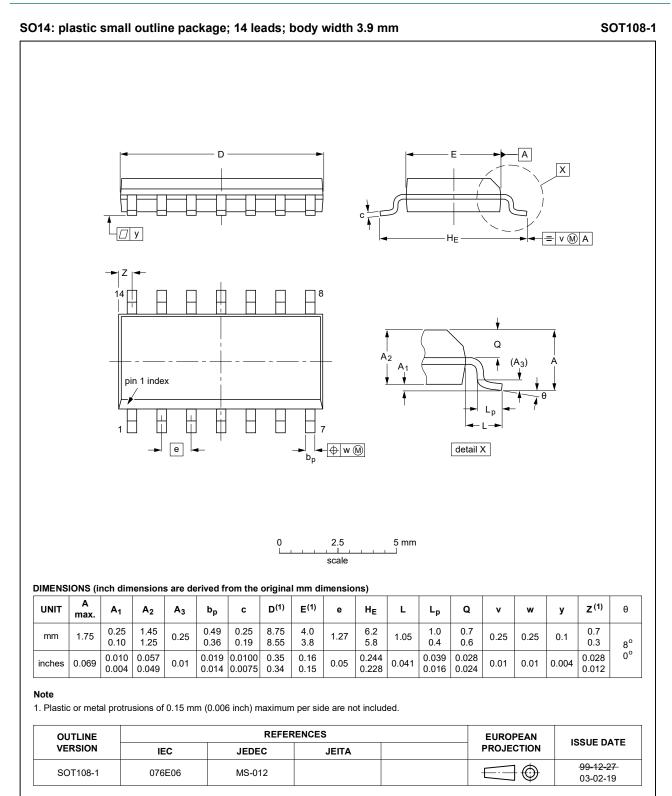
 $C_L$  = load capacitance including jig and probe capacitance.

### Fig. 7. Test circuit for measuring switching times

### Table 9. Test data

Туре	Input Lo		Load	Test
	VI	t <sub>r</sub> , t <sub>f</sub>	CL	
74HC08	V <sub>CC</sub>	6.0 ns	15 pF, 50 pF	t <sub>PLH</sub> , t <sub>PHL</sub>
74HCT08	3.0 V	6.0 ns	15 pF, 50 pF	t <sub>PLH</sub> , t <sub>PHL</sub>

### **11. Package outline**



#### Fig. 8. Package outline SOT108-1 (SO14)

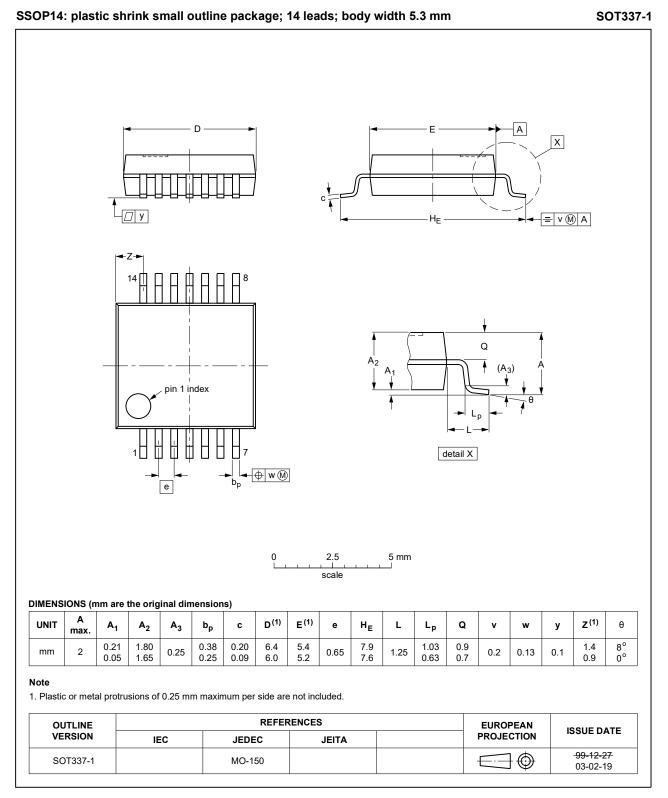


Fig. 9. Package outline SOT337-1 (SSOP14)

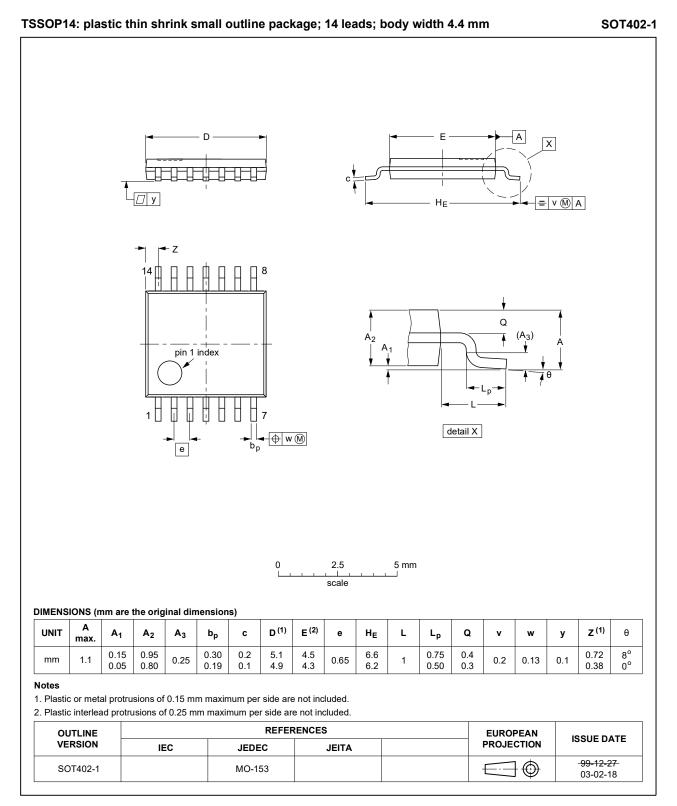


Fig. 10. Package outline SOT402-1 (TSSOP14)

### Quad 2-input AND gate

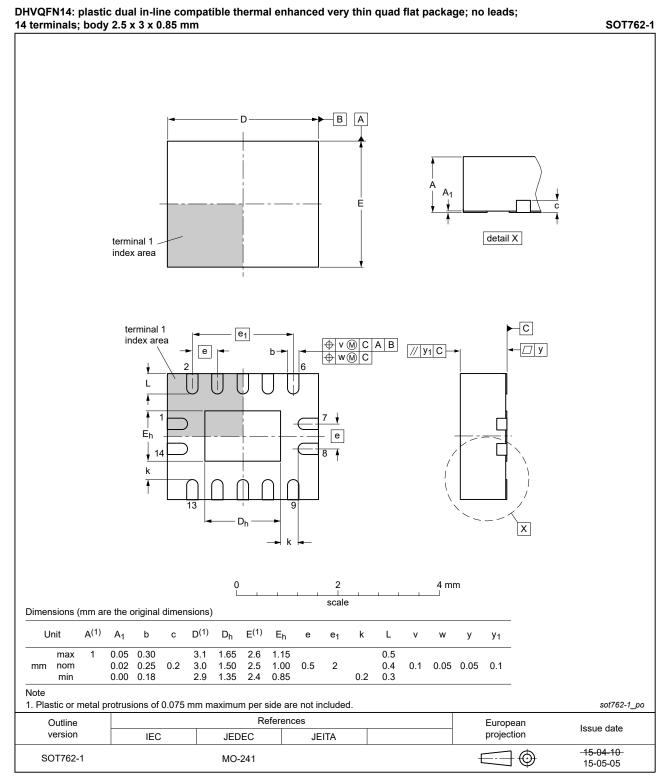


Fig. 11. Package outline SOT762-1 (DHVQFN14)

# 12. Abbreviations

Table 10. Abbreviations					
Acronym	Description				
CMOS	Complementary Metal-Oxide Semiconductor				
DUT	Device Under Test				
ESD	ElectroStatic Discharge				
HBM	Human Body Model				
MM	Machine Model				
TTL	Transistor-Transistor Logic				

# 13. Revision history

### Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes		
74HC_HCT08 v.7	20200416	Product data sheet	-	74HC_HCT08 v.6		
Modifications:	• <u>Table 4</u> : De	• <u>Table 4</u> : Derating values for P <sub>tot</sub> total power dissipation updated.				
74HC_HCT08 v.6	20170613	Product data sheet	-	74HC_HCT08 v.5		
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>					
74HC_HCT08 v.5	20151130	Product data sheet	-	74HC_HCT08 v.4		
Modifications:	Type numbers 74HC08N and 74HCT08N (SOT27-1) removed.					
74HC_HCT08 v.4	20120906	Product data sheet	-	74HC_HCT08 v.3		
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>					
74HC_HCT08 v.3	20030725	Product specification	-	74HC_HCT08_CNV v.2		
74HC_HCT08_CNV v.2	19970826	Product specification	-	-		

# 14. Legal information

#### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

 Please consult the most recently issued document before initiating or completing a design.

- [2] The term 'short data sheet' is explained in section "Definitions".
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