19-4338; Rev A; 9/91

MAXIM

Voltage-Output, 12-Bit DACs with Internal Reference

General Description

The MAX507/MAX508 are complete 12-bit, voltage-output digital-to-analog converters (DACs). The DAC output voltage and the reference have the same polarity, allowing single-supply operation. Both DACs include an internal buried-zener reference. Integrating a DAC, voltage-output amplifier, and reference on one monolithic device greatly enhances reliability over multi-chip circuits.

Double-buffered logic inputs interface easily to microprocessors (μPs). Data is transferred into the input register either from a 12-bit-wide data bus (MAX507) for 16-bit μPs, or in a right-justified (8+4)-bit format (MAX508) for 8- or 16-bit μPs. All logic signals are level triggered and are TTL and CMOS compatible. Interface timing specifications insure compatibility with all common μPs.

The DACs are specified and tested for both dual- and single-supply operation. Usable supplies range from single +12V to dual ±15V.

On-board gain-setting resistors allow three output-voltage ranges: 0V to +5V and 0V to +10V can be generated when using either single or dual supplies. With dual supplies, ±5V is also available. The output amplifier can drive a 2kΩ load to +10V.

Applications

Digital Offset and Gain Adjustment
Industrial Controls
Arbitrary Function Waveform Generators
Automatic Test Equipment
Automated Calibration
Machine and Motion Control

Features

- ♦ 12-Bit Voltage Output
- ♦ Internal Voltage Reference
- ♦ Fast μP Interface
- ♦ 12 (MAX507) and 8+4 (MAX508) Data-Bus Widths
- ♦ Single +12V to Dual ±15V Supply Operation
- ♦ 20- and 24-Pin DIP and Wide SO Packages

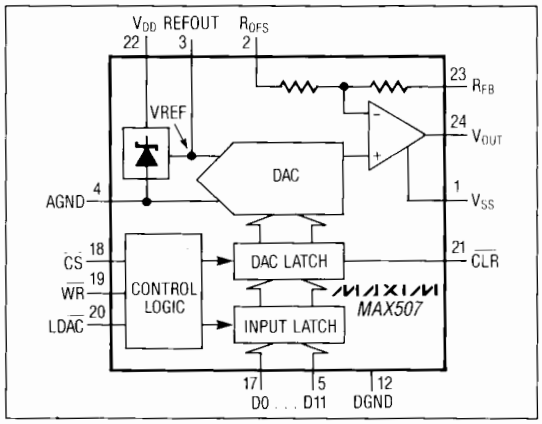
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSBs)
MAX507ACNG	0°C to +70°C	24 Narrow Plastic DIP	±1/2
MAX507BCNG	0°C to +70°C	24 Narrow Plastic DIP	±3/4
MAX507ACWG	0°C to +70°C	24 Wide SO	±1/2
MAX507BCWG	0°C to +70°C	24 Wide SO	±3/4
MAX507BC/D	0°C to +70°C	Dice*	±3/4
MAX507AENG	-40°C to +85°C	24 Narrow Plastic DIP	±1/2
MAX507BENG	-40°C to +85°C	24 Narrow Plastic DIP	±3/4
MAX507AEWG	-40°C to +85°C	24 Wide SO	±1/2
MAX507BEWG	-40°C to +85°C	24 Wide SO	±3/4
MAX507AMRG	-55°C to +125°C	24 Narrow CERDIP**	±1/2
MAX507BMRG	-55°C to +125°C	24 Narrow CERDIP**	±3/4

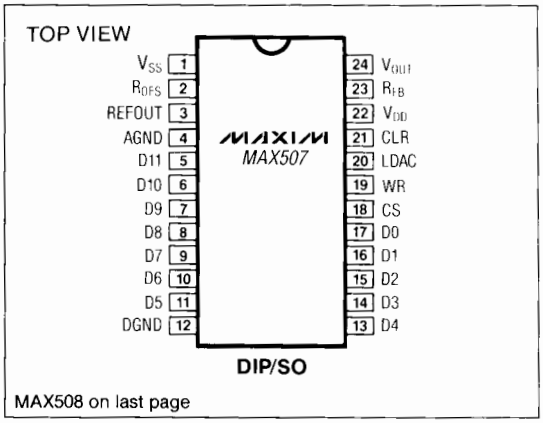
Ordering Information continued on page 12.

* *Contact factory for dice specifications.*
** *Contact factory for availability and processing to MIL-STD-883.*

Functional Diagram



Pin Configurations



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Voltage-Output, 12-Bit DACs with Internal Reference

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND ..... -0.3V, +17V
V_{DD} to DGND ..... -0.3V, +17V
V_{DD} to V_{SS} ..... -0.3V, +34V
AGND to DGND ..... -0.3V, V_{DD}
Digital Input Voltage to GND ..... -0.3V, V_{DD} +0.3V
V_{OUT} to AGND (Note 1) ..... V_{SS}, V_{DD}
V_{OUT} to V_{SS} (Note 1) ..... 0V, +34V
V_{OUT} to V_{DD} (Note 1) ..... -34V, 0V
REFOUT to AGND (Note 1) ..... -0.3V, V_{DD} +0.3V

Continuous Power Dissipation (any package)
to +75°C 450mW
derate above +75°C ..... 6mW/°C
Operating Temperature Ranges:
MAX507_C_, MAX508_C_ ..... 0°C to +70°C
MAX507_E_, MAX508_E_ ..... -40°C to +85°C
MAX507_M_, MAX508_M_ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: The output can be shorted to either supply rail if the package power dissipation is not exceeded. Typical short-circuit current to AGND is 25mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Single Supply (V_{DD} = +11.4V to +15.75V, V_{SS} = AGND = DGND = 0V, R_L = 2kΩ, C_L = 100pF, REFOUT unloaded, all grades, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution	N			12			Bits
Relative Accuracy	INL	T_A = +25°C	MAX507/508A			±1/2	LSB
			MAX507/508B			±3/4	
		T_A = T_{MIN} to T_{MAX}	MAX507/508A			±3/4	
			MAX507/508B			±1	
Differential Nonlinearity	DNL					±1	LSB
Unipolar Offset Error		T_A = +25°C				±3	LSB
		T_A = T_{MIN} to T_{MAX}				±5	
DAC Gain Error						±2	LSB
Full-Scale Output Voltage Error		V_{DD} = +12V or +15V	T_A = +25°C			±0.2	%FSR
			T_A = T_{MIN} to T_{MAX}			±0.6	
Full-Scale Output Voltage Change		V_{DD} over full range	T_A = +25°C			±0.12	%FSR/V
			T_A = T_{MIN} to T_{MAX}			±0.2	
Full-Scale Tempco		MAX507/508_C/E				±30	ppm FSR/°C
		MAX507/508_M				±40	
Unipolar Offset Error Change		V_{DD} = +12V ± 5% or +15V ± 5%				±1	mV

ELECTRICAL CHARACTERISTICS (continued)

Single Supply (V_{DD} = +11.4V to +15.75V, V_{SS} = AGND = DGND = 0V, R_L = 2kΩ, C_L = 100pF, REFOUT unloaded, all grades, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE							
Reference Output		V_{DD} = +12V or +15V	T_A = +25°C	4.99		5.01	V
Reference Voltage Change		V_{DD} = +12V ± 5% or +15V ± 5%	T_A = +25°C			2	mV/V
			T_A = T_{MIN} to T_{MAX}			6	
Reference Temperature Coefficient		MAX507/508_C/E			±30		ppm/°C
		MAX507/508_M			±40		
Reference Load Sensitivity		I_{LOAD} = 0μA to 100μA				±1	mV
ANALOG OUTPUT							
Ranges (Note 2)						0 to 5	V
						0 to 10	
Output Range Resistors				15		30	kΩ
DC Output Impedance					0.5		Ω
Short-Circuit Current					40		mA
DYNAMIC PERFORMANCE (Note 3)							
Voltage-Output Slew Rate				2			V/μs
V_{OUT} Settling Time		To ±1/2 LSB for full-scale change				5	μs
Digital Feedthrough					10		nV-s
Digtal-to-Analog Glitch Impulse		Major carry transition			30		nV-s
Output Load Resistance (Note 2)		V_{OUT} = 0V to +10V		2			kΩ
POWER SUPPLIES							
V_{DD} Range		For specified performance		11.4		15.75	V
I_{DD}		Outputs unloaded	T_A = +25°C			9	mA
			T_A = T_{MIN} to T_{MAX}			12	

Voltage-Output, 12-Bit DACs with Internal Reference

ELECTRICAL CHARACTERISTICS

Dual Supply (V_{DD} = +11.4V to +15.75V, V_{SS} = -11.4V to -15.75V, DGND = AGND = 0V, R_L = 2kΩ, C_L = 100pF, REFOUT unloaded, all grades, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution	N			12			Bits
Relative Accuracy	INL	T_A = +25°C	MAX507/508A			±1/2	LSB
			MAX507/508B			±3/4	
		T_A = T_{MIN} to T_{MAX}	MAX507/508A			±3/4	
			MAX507/508B			±1	
Differential Nonlinearity	DNL					±1	LSB
Bipolar Zero Offset Error	BZOE	MAX507/508A	T_A = +25°C			±2	LSB
			T_A = T_{MIN} to T_{MAX}			±4	
		MAX507/508B	T_A = +25°C			±3	
			T_A = T_{MIN} to T_{MAX}			±5	
DAC Gain Error						±2	LSB
Full-Scale Output Voltage Error		V_{DD} = +15V, V_{SS} = -15V	T_A = +25°C			±0.2	%FSR
			T_A = T_{MIN} to T_{MAX}			±0.6	
		V_{DD} = +12V, V_{SS} = -12V	T_A = +25°C			±0.2	
			T_A = T_{MIN} to T_{MAX}			±0.6	
Full-Scale Output Change with V_{DD}		V_{DD} = +12V ± 5% or +15V ± 5%, V_{SS} = -12V or -15V	T_A = +25°C			±0.12	%FSR/V
			T_A = T_{MIN} to T_{MAX}			±0.2	
Full-Scale Output Change with V_{SS}	V_{SS}	V_{SS} = -12V ± 5% or -15V ± 5%, V_{DD} = +12V or +5V				0.01	%FSR/V
Full-Scale Tempco		MAX507/508_C/E				±30	ppm FSR/°C
		MAX507/508_M				±40	
Bipolar Zero Offset Change		V_{DD} = +12V ± 5% or +15V ± 5%, V_{SS} = -12V or -15V				±1	mV
		V_{SS} = -12V ± 5% or -15V ± 5%, V_{DD} = +12V or +15V				±1	
REFERENCE							
Reference Output		V_{DD} = +12V or +15V	T_A = +25°C	4.99		5.01	V
Reference Output Change		V_{DD} over full range	T_A = +25°C			2	mV/V
			T_A = T_{MIN} to T_{MAX}			6	
Reference Temperature Coefficient		MAX507/508_C/E			±30		ppm/°C
		MAX507/508_M			±40		
Reference Load Sensitivity		I_{LOAD} = 0μA to 100μA				±1	mV

ELECTRICAL CHARACTERISTICS (continued)

Dual Supply (V_{DD} = +11.4V to +15.75V, V_{SS} = -11.4V to -15.75V, DGND = AGND = 0V, R_L = 2kΩ, C_L = 100pF, REFOUT unloaded, all grades, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG OUTPUT							
Ranges (Notes 2, 4)					0 to +5 or +10, -5 to +5		V
Output Range Resistors				15		30	kΩ
DC Output Impedance					0.5		Ω
Short-Circuit Current					40		mA
DYNAMIC PERFORMANCE (Note 3)							
Voltage-Output Slew Rate				2			V/μs
V_{OUT} Settling Time		to ±1/2 LSB				5	μs
Digital Feedthrough					10		nV-s
Digtal-to-Analog Glitch Impulse		Major carry transition			30		nV-s
Output Load Resistance		V_{OUT} = -5V to +10V		2			kΩ
POWER SUPPLIES							
V_{DD} Range		For specified performance		11.4		15.75	V
V_{SS} Range		For specified performance		-11.4		-15.75	V
I_{DD}		Outputs unloaded	T_A = +25°C			9	mA
			T_A = T_{MIN} to T_{MAX}			12	
I_{SS}		Outputs unloaded	T_A = +25°C			3	mA
			T_A = T_{MIN} to T_{MAX}			5	

Voltage-Output, 12-Bit DACs with Internal Reference

ELECTRICAL CHARACTERISTICS

Single or Dual Supply (V_{DD} = +11.4V to +15.75V, V_{SS} = 0V to -15.75V, DGND = AGND = 0V, REFOUT unloaded, R_L = 2kΩ, C_L = 100pF, all grades, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL INPUTS							
V_{INH}				2.4			V
V_{INL}						0.8	V
Input Current	I_{IN}	D0-D11	T_A = +25°C			±1	µA
			T_A = T_{MIN} to T_{MAX}			±10	
I_{INH}		$\overline{CS}$, $\overline{WR}$, $\overline{LDAC}$, $\overline{CLR}$	T_A = +25°C			±1	µA
			T_A = T_{MIN} to T_{MAX}			±10	
I_{INL}		$\overline{CS}$, $\overline{WR}$, $\overline{LDAC}$, $\overline{CLR}$	T_A = +25°C			±150	µA
			T_A = T_{MIN} to T_{MAX}			±200	
Digital Input Capacitance					8		pF

TIMING CHARACTERISTICS

(All grades, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ Pulse Width (Note 5)	t_1	T_A = +25°C	80			ns
		T_A = T_{MIN} to T_{MAX}	100			
$\overline{WR}$ Pulse Width	t_2	T_A = +25°C	80			ns
		T_A = T_{MIN} to T_{MAX}	100			
$\overline{CS}$ to $\overline{WR}$ Setup Time (Note 5)	t_3		0			ns
$\overline{CS}$ to $\overline{WR}$ Hold Time (Note 5)	t_4		0			ns
Data to $\overline{WR}$ Setup Time	t_5	T_A = +25°C	100			ns
		T_A = T_{MIN} to T_{MAX}	110			
Data to $\overline{WR}$ Hold Time	t_6		10			ns
$\overline{LDAC}$ Pulse Width	t_7	T_A = +25°C	80			ns
		T_A = T_{MIN} to T_{MAX}	100			
$\overline{CLR}$ Pulse Width (MAX507)	t_8	T_A = +25°C	80			ns
		T_A = T_{MIN} to T_{MAX}	100			

Note 2: V_{OUT} must be less than (V_{DD} - 2.5V).
Note 3: Dynamic performance is included for design guidance, not subject to test.
Note 4: The 0V to +5V or +10V ranges can be used with V_{SS} = -5V with no degradation.
Note 5: $\overline{CS}$ = $\overline{CS}$LSB and $\overline{CS}$MSB for MAX508.

Detailed Description

Digital-to-Analog Converters

The MAX507/MAX508 are 12-bit, voltage-output DACs. The DAC output voltage has the same polarity as the reference, allowing single-supply operation.

The basic DAC circuit consists of a laser-trimmed, thin-film, R-2R resistor array with NMOS voltage switches (Figure 1).

Output-Buffer Amplifier

The output amplifier is noninverting and configurable for a gain of 1 or 2. Three output voltage ranges can be configured for: 0V to +5V, 0V to +10V, and -5V to +5V. The output amplifier can drive 2kΩ in parallel with 100pF connected to GND.

The MAX507/MAX508 can operate from a single supply with a 0V to +5V or a 0V to +10V output range by tying V_{SS} to 0V. However, the speed and current-sinking capability of the amplifier decreases as the output falls within 0.5V of V_{SS}. Speed and current-sinking capability can be maintained by including a negative supply. Table 1 lists the allowable single and dual supplies for each range.

The output amplifier's small-signal bandwidth is typically 2MHz. Output noise is approximately $25nV/\sqrt{Hz}$ at 1kHz, and output broadband noise is approximately $25\mu V_{RMS}$.

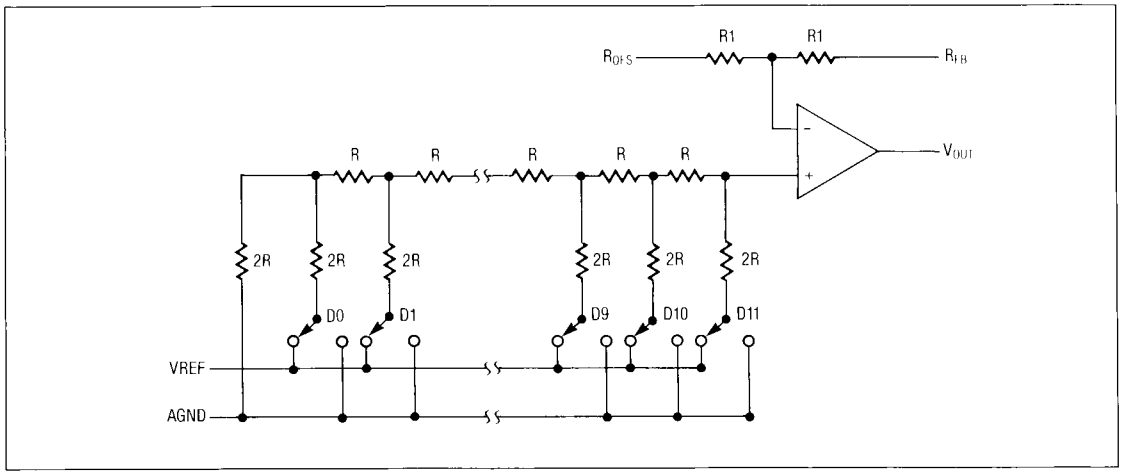


Figure 1. Simplified MAX507 DAC Circuit

Table 1. Output Voltage Range vs. Supply Voltage

Range	Single Supply V_{DD}	Dual Supply V_{DD}	Dual Supply V_{SS}
0V to +5V	+11.4V to +15.75V	+11.4V to +15.75V	-4.5V to -15.75V
0V to +10V	+14.25V to +15.75V	+14.25V to +15.75V	-4.5V to -15.75V
-5V to +5V		+11.4V to +15.75V	-11.4V to -15.75V

Voltage-Output, 12-Bit DACs with Internal Reference

Voltage Reference

The voltage at REFOUT is 5V ± 10mV at +25°C. The reference is internally connected to the DAC and is buffered to accommodate the DAC's variable impedance. This buffer is capable of driving the DAC, the R_{OFS} resistor, and up to 500μA of external current. MAX507/MAX508 specifications are determined with the internal reference. The reference should be decoupled at REFOUT with 10Ω in series with the recommended decoupling capacitors, 10μF in parallel with 0.1μF.

Digital Inputs and Interface Logic

All logic inputs are compatible with both TTL and 5V CMOS logic. Supply current is specified for TTL input levels, but is reduced by about 450μA when the data inputs are driven near DGND or V_{DD}. The control inputs (CLR, LDAC, WR, CS, CSMSB, and CSLSB) each draw 100μA from I_{DD} when low.

MAX507 Interface

Table 2 is the MAX507 truth table. The MAX507 accepts a 12-bit input word that can be latched or transferred directly to the DAC. CS and WR control the input latch, and LDAC transfers information from the input latch to the DAC latch.

Table 2. MAX507 Truth Table

CLR	LDAC	WR	CS	Function
1	0	0	0	Both latches transparent
1	1	1	X	Both latches latched
1	1	X	1	Both latches latched
1	1	0	0	Input latch transparent
1	1	↑	0	Input latch latched
1	0	1	1	DAC latch transparent
1	↑	1	1	DAC latch latched
0	X	X	X	DAC latch all 0s
↑	1	1	1	DAC latch latched with 0s; output at 0V or -5V
↑	0	0	0	Both latches transparent; output follows input data

1 = High State X = Don't Care
0 = Low State ↑ = Rising Edge

The input latch is transparent when CS and WR are low; the DAC latch is transparent when LDAC is low. Data is latched within the input latch on the rising edge of WR when CS is low. The rising edge of LDAC latches data into the DAC when CS and WR are low. After CS and WR are high, LDAC must be held low for t_7 or longer (Figure 2).

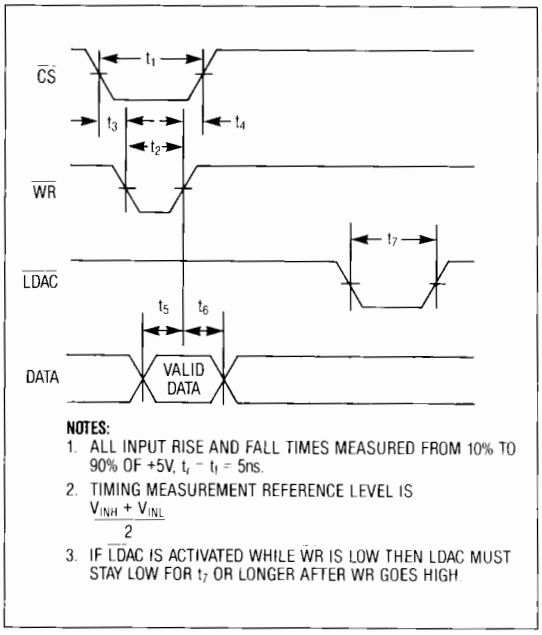


Figure 2. MAX507 Timing Diagram

The DAC latch is reset to zeros with CLR low. CLR acts as a zero override when the input latch and DAC latch are transparent. Then, a low-to-high CLR transition loads all zeros into the DAC latch, and the output remains low (0V to -5V).

MAX508 Interface

The MAX508's 8-bit-wide data bus interfaces with 8-bit μPs. The MAX508 contains an input latch and a DAC latch. The data held in the DAC latch determines the output of the DAC. Table 3 is the MAX508 truth table, Figure 3 shows the input control logic, and Figure 4 shows the write-cycle timing.

Table 3. MAX508 Truth Table

$\overline{CSLSB}$	$\overline{CSMSB}$	$\overline{WR}$	$\overline{LDAC}$	Function
0	1	0	1	Loads LSBs to input latches
0	1	↑	1	Locks LSBs in input latches
↑	1	0	1	Locks LSBs in input latches
1	0	0	1	Loads MSBs to input latches
1	0	↑	1	Locks MSBs in input latches
1	↑	0	1	Locks MSBs in input latches
1	1	1	0	Loads input into DAC latch
1	1	1	↑	Locks input into DAC latch
1	0	0	0	Loads MSBs to input latches and loads input into DAC latch
1	1	1	1	No data transfer

1 = High State 0 = Low State ↑ = Rising Edge

Right-justified data is loaded into the MAX508 using $\overline{CSMSB}$, $\overline{CSLSB}$, and $\overline{WR}$. Data can be latched into the input latch on the rising edge of $\overline{WR}$ for the most significant bit (MSB) and least significant bit (LSB), or on the rising edge of $\overline{CSMSB}$ for the MSB and $\overline{CSLSB}$ for the LSB. Either the MSB or the LSB can be loaded first.

The complete, 12-bit word loads into the DAC register when $\overline{LDAC}$ is low, and latches on $\overline{LDAC}$'s rising edge. $\overline{LDAC}$ is asynchronous and independent of $\overline{WR}$, so it is ideal for simultaneously updating multiple MAX508 outputs. Because $\overline{LDAC}$ can occur during a write cycle, it must stay low for t_7 (or longer) after $\overline{WR}$ goes high to ensure correct data is latched to the output.

The MAX508 output can be updated in two write cycles by tying $\overline{CSMSB}$ and $\overline{LDAC}$. In this automatic transfer mode, $\overline{CSLSB}$ and $\overline{WR}$ latch the lower 8 bits into the input latch; then $\overline{CSMSB}$, $\overline{WR}$, and $\overline{LDAC}$ load the upper 4 bits into the input latch and transfer the 12-bit word into the DAC latch. Alternatively, the MAX507 can be updated in two writes by tying $\overline{CSLSB}$ to $\overline{LDAC}$ if the upper 4 bits are input first, followed by the lower 8 bits.

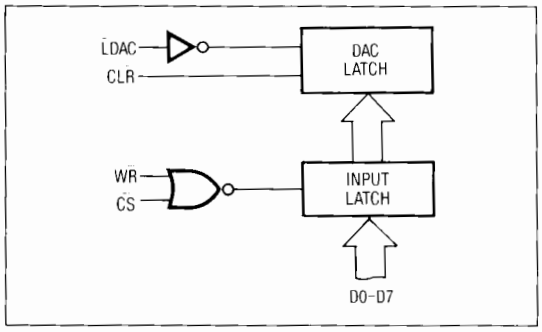


Figure 3a. MAX507 Input Control Logic

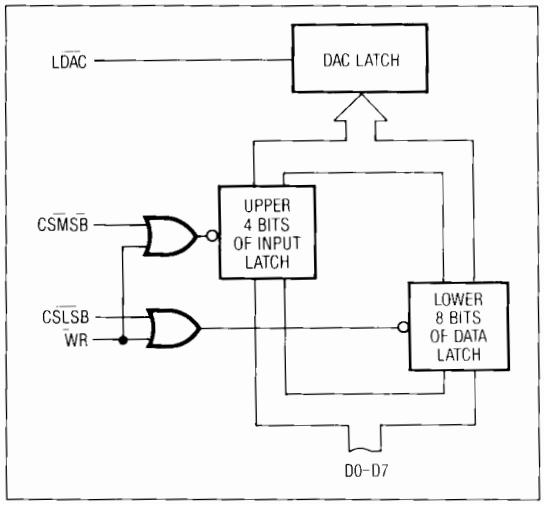


Figure 3b. MAX508 Input Control Logic

Voltage-Output, 12-Bit DACs with Internal Reference

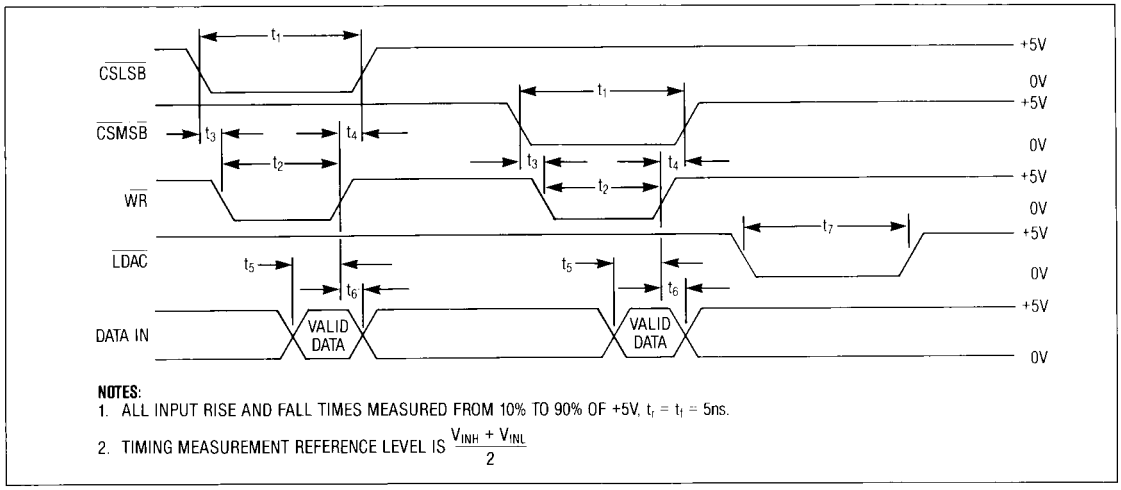


Figure 4. MAX508 Timing Diagram

Unipolar Configuration

The MAX507/MAX508 are set up for a 0V to +5V unipolar output range by connecting R_{OFS}, R_{FB}, and V_{OUT} (Figure 5). The converters operate from either a single or a dual supply in this configuration. See Table 4 for the DAC-latch contents (input) vs. analog output (output). In this range, 1LSB = VREF (2^{-12}).

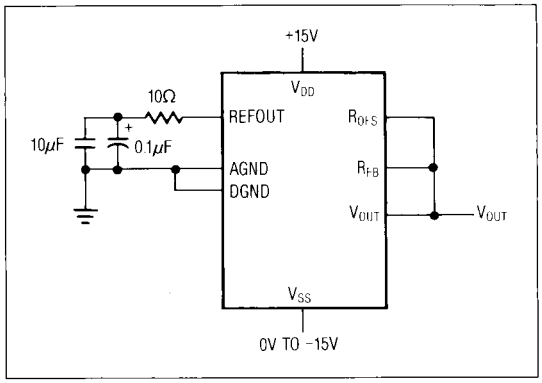


Figure 5. Unipolar Configuration (0V to +5V Output)

Table 4. Unipolar-Code Table (0V to +5V Output)

INPUT			OUTPUT
1111	1111	1111	(VREF) 4095/4096
1000	0000	0001	(VREF) 2049/4096
1000	0000	0000	(VREF) 2048/4096 =+VREF/2
0111	1111	1111	(VREF) 2047/4096
0000	0000	0001	(VREF) 1/4096
0000	0000	0000	0V

A 0V to +10V unipolar output range is set up by connecting R_{OFS} to AGND and R_{FB} to V_{OUT} (Figure 6). See Table 5 for the DAC-latch contents (input) vs. analog output (output). The MAX507/MAX508 operate from either a single or a dual supply in this configuration. In this range, 1LSB = VREF (2^{-11}).

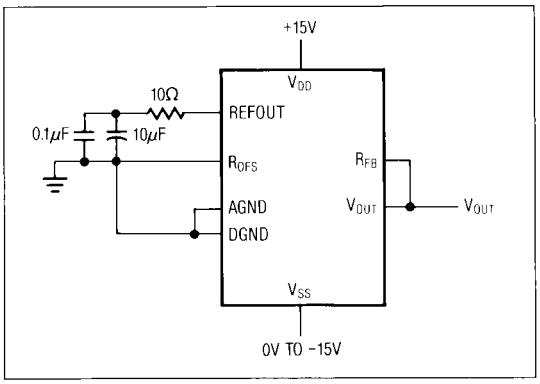


Figure 6. Unipolar Configuration (0V to +10V Output)

Table 5. Unipolar-Code Table (0V to +10V Output)

INPUT			OUTPUT
1111	1111	1111	$+2\ (VREF)\frac{4095}{4096}$
1000	0000	0001	$+2\ (VREF)\frac{2049}{4096}$
1000	0000	0000	$+2\ (VREF)\frac{2048}{4096} = +VREF$
0111	1111	1111	$+2\ (VREF)\frac{2047}{4096}$
0000	0000	0001	$+2\ (VREF)\frac{1}{4096}$
0000	0000	0000	0V

Bipolar Configuration

A -5V to +5V bipolar range is set up by connecting R_{OFS} to REFOUT and R_{FB} to V_{OUT}, and operating from dual power supplies (Table 1). See Table 6 for the DAC-latch contents (input) vs. analog output (output). In this range, 1LSB = (2) VREF (2^{-11}) = (VREF) 1/2048.

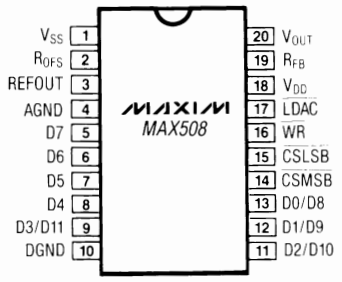
Table 6. Bipolar-Code Table (-5V to +5V Output)

INPUT			OUTPUT
1111	1111	1111	$(+VREF)\frac{2047}{2048}$
1000	0000	0001	$(+VREF)\frac{1}{2048}$
1000	0000	0000	0V
0111	1111	1111	$(-VREF)\frac{1}{2048}$
0000	0000	0001	$(-VREF)\frac{2047}{2048}$
0000	0000	0000	$(-VREF)\frac{2048}{2048} = -VREF$

Voltage-Output, 12-Bit DACs with Internal Reference

Pin Configurations (continued)

TOP VIEW



DIP/SO

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSBs)
MAX508ACPP	0°C to +70°C	20 Narrow Plastic DIP	±1/2
MAX508BCPP	0°C to +70°C	20 Narrow Plastic DIP	±3/4
MAX508ACWP	0°C to +70°C	20 Wide SO	±1/2
MAX508BCWP	0°C to +70°C	20 Wide SO	±3/4
MAX508BC/D	0°C to +70°C	Dice*	±3/4
MAX508AEPP	-40°C to +85°C	20 Narrow Plastic DIP	±1/2
MAX508BEPP	-40°C to +85°C	20 Narrow Plastic DIP	±3/4
MAX508AEWP	-40°C to +85°C	20 Wide SO	±1/2
MAX508BEWP	-40°C to +85°C	20 Wide SO	±3/4
MAX508AMJP	-55°C to +125°C	20 Narrow CERDIP**	±1/2
MAX508BMJP	-55°C to +125°C	20 Narrow CERDIP**	±3/4

* *Contact factory for dice specifications.*
** *Contact factory for availability and processing to MIL-STD-883.*

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