3-Channel, Low Noise, Low Power, 16-/24-Bit Σ-Δ ADC with On-Chip In-Amp and Reference

AD7792/AD7793

FEATURES

Up to 23 bits effective resolution
RMS noise
40 nV @ 4.17 Hz
85 nV @ 16.7 Hz
Current: 400 µA typical
Power-down: 1 µA maximum
Low noise programmable gain instrumentation amp
Band gap reference with 4 ppm/°C drift typical
Update rate: 4.17 Hz to 470 Hz
3 differential inputs
Internal clock oscillator
Simultaneous 50 Hz/60 Hz rejection
Programmable current sources
On-chip bias voltage generator
Burnout currents
Power supply: 2.7 V to 5.25 V
–40°C to +105°C temperature range
Independent interface power supply
16-lead TSSOP package
Interface
- **3-wire serial**
- **SPI®, QSPI™, MICROWIRE™, and DSP compatible**
- **Schmitt trigger on SCLK**

APPLICATIONS

Thermocouple measurements
RTD measurements
Thermistor measurements
Gas analysis
Industrial process control
Instrumentation
Portable instrumentation
Blood analysis
Smart transmitters
Liquid/gas chromatography
6-digit DVM

FUNCTIONAL BLOCK DIAGRAM

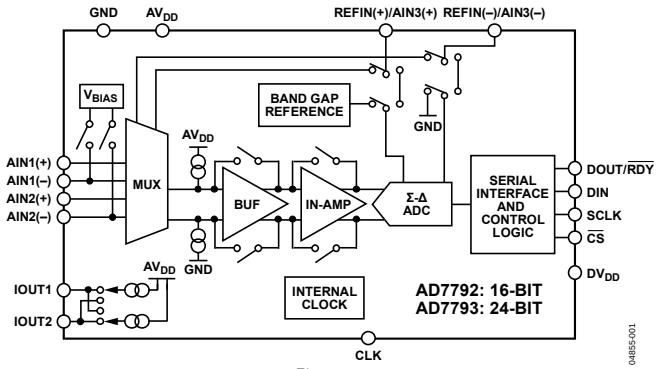

Figure 1.

GENERAL DESCRIPTION

The AD7792/AD7793 are low power, low noise, complete analog front ends for high precision measurement applications. The AD7792/AD7793 contain a low noise 16-/24-bit Σ-Δ ADC with three differential analog inputs. The on-chip, low noise instrumentation amplifier means that signals of small amplitude can be interfaced directly to the ADC. With a gain setting of 64, the rms noise is 40 nV when the update rate equals 4.17 Hz.

The devices contain a precision low noise, low drift internal band gap reference and can accept an external differential reference. Other on-chip features include programmable excitation current sources, burnout currents, and a bias voltage generator. The bias voltage generator sets the common-mode voltage of a channel to $AV_{DD}/2$.

The devices can be operated with either the internal clock or an external clock. The output data rate from the parts is software-programmable and can be varied from 4.17 Hz to 470 Hz.

The parts operate with a power supply from 2.7 V to 5.25 V. They consume a current of 400 µA typical and are housed in a 16-lead TSSOP package.

Rev. B

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SPECIFICATIONS

AV_{DD} = 2.7 V to 5.25 V; DV_{DD} = 2.7 V to 5.25 V; GND = 0 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	AD7792B/AD7793B[1]	Unit	Test Conditions/Comments
ADC CHANNEL			
Output Update Rate	4.17 to 470	Hz nom	
No Missing Codes[2]	24	Bits min	f_{ADC} < 242 Hz, AD7793
	16	Bits min	AD7792
Resolution			See Output Noise and Resolution Specifications
Output Noise and Update Rates			See Output Noise and Resolution Specifications
Integral Nonlinearity	±15	ppm of FSR max	
Offset Error[3]	±1	µV typ	
Offset Error Drift vs. Temperature[4]	±10	nV/°C typ	
Full-Scale Error[3, 5]	±10	µV typ	
Gain Drift vs. Temperature[4]	±1	ppm/°C typ	Gain = 1 to 16, external reference
	±3	ppm/°C typ	Gain = 32 to 128, external reference
Power Supply Rejection	100	dB min	AIN = 1 V/gain, gain ≥ 4, external reference
ANALOG INPUTS			
Differential Input Voltage Ranges	$\pm V_{REF}$/Gain	V nom	V_{REF} = REFIN(+) − REFIN(−) or internal reference, gain = 1 to 128
Absolute AIN Voltage Limits[2]			
Unbuffered Mode	GND − 30 mV	V min	Gain = 1 or 2
	AV_{DD} + 30 mV	V max	
Buffered Mode	GND + 100 mV	V min	Gain = 1 or 2
	AV_{DD} − 100 mV	V max	
In-Amp Active	GND + 300 mV	V min	Gain = 4 to 128
	AV_{DD} − 1.1	V max	
Common-Mode Voltage, V_{CM}	0.5	V min	V_{CM} = (AIN(+) + AIN(−))/2, gain = 4 to 128
Analog Input Current			
Buffered Mode or In-Amp Active			
Average Input Current[2]	±1	nA max	Gain = 1 or 2, update rate < 100 Hz
	±250	pA max	Gain = 4 to 128, update rate < 100 Hz
Average Input Current Drift	±2	pA/°C typ	
Unbuffered Mode			Gain = 1 or 2.
Average Input Current	±400	nA/V typ	Input current varies with input voltage
Average Input Current Drift	±50	pA/V/°C typ	
Normal Mode Rejection[2]			
Internal Clock			
@ 50 Hz, 60 Hz	65	dB min	80 dB typ, 50 ± 1 Hz, 60 ± 1 Hz, FS[3:0] = 1010[6]
@ 50 Hz	80	dB min	90 dB typ, 50 ± 1 Hz, FS[3:0] = 1001[6]
@ 60 Hz	90	dB min	100 dB typ, 60 ± 1 Hz, FS[3:0] = 1000[6]
External Clock			
@ 50 Hz, 60 Hz	80	dB min	90 dB typ, 50 ± 1 Hz, 60 ± 1 Hz, FS[3:0] = 1010[6]
@ 50 Hz	94	dB min	100 dB typ, 50 ± 1 Hz, FS[3:0] = 1001[6]
@ 60 Hz	90	dB min	100 dB typ, 60 ± 1 Hz, FS[3:0] = 1000[6]
Common-Mode Rejection			
@ DC	100	dB min	AIN = 1 V/gain, gain ≥ 4
@ 50 Hz, 60 Hz[2]	100	dB min	50 ± 1 Hz, 60 ± 1 Hz, FS[3:0] = 1010[6]
@ 50 Hz, 60 Hz[2]	100	dB min	50 ± 1 Hz (FS[3:0] = 1001)[6], 60 ± 1 Hz (FS[3:0] = 1000)[6]

Parameter	AD7792B/AD7793B[1]	Unit	Test Conditions/Comments
REFERENCE			
Internal Reference			
Internal Reference Initial Accuracy	1.17 ± 0.01%	V min/max	AV_{DD} = 4 V, T_A = 25°C
Internal Reference Drift[2]	4	ppm/°C typ	
	15	ppm/°C max	
Power Supply Rejection	85	dB typ	
External Reference			
External REFIN Voltage	2.5	V nom	REFIN = REFIN(+) − REFIN(−)
Reference Voltage Range[2]	0.1	V min	
	AV_{DD}	V max	When V_{REF} = AV_{DD}, the differential input must be limited to 0.9 × V_{REF} /gain if the in-amp is active
Absolute REFIN Voltage Limits[2]	GND − 30 mV	V min	
	AV_{DD} + 30 mV	V max	
Average Reference Input Current	400	nA/V typ	
Average Reference Input Current Drift	±0.03	nA/V/°C typ	
Normal Mode Rejection	Same as for analog inputs		
Common-Mode Rejection	100	dB typ	
EXCITATION CURRENT SOURCES			
(IEXC1 and IEXC2)			
Output Current	10/210/1000	µA nom	
Initial Tolerance at 25°C	±5	% typ	
Drift	200	ppm/°C typ	
Current Matching	±0.5	% typ	Matching between IEXC1 and IEXC2; V_{OUT} = 0 V
Drift Matching	50	ppm/°C typ	
Line Regulation (V_{DD})	2	%/V typ	AV_{DD} = 5 V ± 5%
Load Regulation	0.2	%/V typ	
Output Compliance	AV_{DD} − 0.65	V max	10 µA or 210 µA currents selected
	AV_{DD} − 1.1	V max	1 mA currents selected
	GND − 30 mV	V min	
TEMPERATURE SENSOR			
Accuracy	±2	°C typ	Applies if user calibrates the temperature sensor
Sensitivity	0.81	mV/°C typ	
BIAS VOLTAGE GENERATOR			
V_{BIAS}	AV_{DD}/2	V nom	
V_{BIAS} Generator Start-Up Time	See Figure 10	ms/nF typ	Dependent on the capacitance on the AIN pin
INTERNAL/EXTERNAL CLOCK			
Internal Clock			
Frequency[2]	64 ± 3%	kHz min/max	
Duty Cycle	50:50	% typ	
External Clock			
Frequency	64	kHz nom	A 128 kHz external clock can be used if the divide-by-2 function is used (Bit CLK1 = CLK0 = 1)
Duty Cycle	45:55 to 55:45	% typ	Applies for external 64 kHz clock; a 128 kHz clock can have a less stringent duty cycle
LOGIC INPUTS			
$\overline{CS}$[2]			
V_{INL}, Input Low Voltage	0.8	V max	DV_{DD} = 5 V
	0.4	V max	DV_{DD} = 3 V
V_{INH}, Input High Voltage	2.0	V min	DV_{DD} = 3 V or 5 V

Parameter	AD7792B/AD7793B[1]	Unit	Test Conditions/Comments
SCLK, CLK, and DIN (Schmitt-Triggered Input)[2]			
$V_T(+)$	1.4/2	V min/V max	DV_{DD} = 5 V
$V_T(-)$	0.8/1.7	V min/V max	DV_{DD} = 5 V
$V_T(+) - V_T(-)$	0.1/0.17	V min/V max	DV_{DD} = 5 V
$V_T(+)$	0.9/2	V min/V max	DV_{DD} = 3 V
$V_T(-)$	0.4/1.35	V min/V max	DV_{DD} = 3 V
$V_T(+) - V_T(-)$	0.06/0.13	V min/V max	DV_{DD} = 3 V
Input Currents	±10	µA max	V_{IN} = DV_{DD} or GND
Input Capacitance	10	pF typ	All digital inputs
LOGIC OUTPUTS (INCLUDING CLK)			
V_{OH}, Output High Voltage[2]	DV_{DD} − 0.6	V min	DV_{DD} = 3 V, I_{SOURCE} = 100 µA
V_{OL}, Output Low Voltage[2]	0.4	V max	DV_{DD} = 3 V, I_{SINK} = 100 µA
V_{OH}, Output High Voltage[2]	4	V min	DV_{DD} = 5 V, I_{SOURCE} = 200 µA
V_{OL}, Output Low Voltage[2]	0.4	V max	DV_{DD} = 5 V, I_{SINK} = 1.6 mA (DOUT/$\overline{RDY}$)/800 µA (CLK)
Floating-State Leakage Current	±10	µA max	
Floating-State Output Capacitance	10	pF typ	
Data Output Coding	Offset binary		
SYSTEM CALIBRATION[2]			
Full-Scale Calibration Limit	+1.05 × FS	V max	
Zero-Scale Calibration Limit	−1.05 × FS	V min	
Input Span	0.8 × FS	V min	
	2.1 × FS	V max	
POWER REQUIREMENTS[7]			
Power Supply Voltage			
AV_{DD} to GND	2.7/5.25	V min/max	
DV_{DD} to GND	2.7/5.25	V min/max	
Power Supply Currents			
I_{DD} Current	140	µA max	110 µA typ @ AV_{DD} = 3 V, 125 µA typ @ AV_{DD} = 5 V, unbuffered mode, external reference
	185	µA max	130 µA typ @ AV_{DD} = 3 V, 165 µA typ @ AV_{DD} = 5 V, buffered mode, gain = 1 or 2, external reference
	400	µA max	300 µA typ @ AV_{DD} = 3 V, 350 µA typ @ AV_{DD} = 5 V, gain = 4 to 128, external reference
	500	µA max	400 µA typ @ AV_{DD} = 3 V, 450 µA typ @ AV_{DD} = 5 V, gain = 4 to 128, internal reference
I_{DD} (Power-Down Mode)	1	µA max	

[1] Temperature range is −40°C to +105°C. At the 19.6 Hz and 39.2 Hz update rates, the INL, power supply rejection (PSR), common-mode rejection (CMR), and normal mode rejection (NMR) do not meet the data sheet specification if the voltage on the AIN(+) or AIN(−) pins exceed AV_{DD} − 16 V typically. When this voltage is exceeded, the INL, for example, is reduced to 18 ppm of FS typically while the PSR is reduced to 69 dB typically. Therefore, for guaranteed performance at these update rates, the absolute voltage on the analog input pins needs to be below AV_{DD} − 1.6 V.
[2] Specification is not production tested, but is supported by characterization data at initial product release.
[3] Following a calibration, this error is in the order of the noise for the programmed gain and update rate selected.
[4] Recalibration at any temperature removes these errors.
[5] Full-scale error applies to both positive and negative full-scale and applies at the factory calibration conditions (AV_{DD} = 4 V, gain = 1, T_A = 25°C).
[6] FS[3:0] are the four bits used in the mode register to select the output word rate.
[7] Digital inputs equal to DV_{DD} or GND with excitation currents and bias voltage generator disabled.

TIMING CHARACTERISTICS

AV_{DD} = 2.7 V to 5.25 V, DV_{DD} = 2.7 V to 5.25 V, GND = 0 V, Input Logic 0 = 0 V, Input Logic 1 = DV_{DD}, unless otherwise noted.

Table 2.

Parameter[1, 2]	Limit at T_{MIN}, T_{MAX} (B Version)	Unit	Conditions/Comments
t_3	100	ns min	SCLK high pulse width
t_4	100	ns min	SCLK low pulse width
Read Operation			
t_1	0	ns min	$\overline{CS}$ falling edge to DOUT/$\overline{RDY}$ active time
	60	ns max	DV_{DD} = 4.75 V to 5.25 V
	80	ns max	DV_{DD} = 2.7 V to 3.6 V
t_2[3]	0	ns min	SCLK active edge to data valid delay[4]
	60	ns max	DV_{DD} = 4.75 V to 5.25 V
	80	ns max	DV_{DD} = 2.7 V to 3.6 V
t_5[5, 6]	10	ns min	Bus relinquish time after $\overline{CS}$ inactive edge
	80	ns max	
t_6	0	ns min	SCLK inactive edge to $\overline{CS}$ inactive edge
t_7	10	ns min	SCLK inactive edge to DOUT/$\overline{RDY}$ high
Write Operation			
t_8	0	ns min	$\overline{CS}$ falling edge to SCLK active edge setup time[4]
t_9	30	ns min	Data valid to SCLK edge setup time
t_{10}	25	ns min	Data valid to SCLK edge hold time
t_{11}	0	ns min	$\overline{CS}$ rising edge to SCLK edge hold time

[1] Sample tested during initial release to ensure compliance. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of DV_{DD}) and timed from a voltage level of 1.6 V.
[2] See Figure 3 and Figure 4.
[3] These numbers are measured with the load circuit shown in Figure 2 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.
[4] SCLK active edge is falling edge of SCLK.
[5] These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit shown in Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and, as such, are independent of external bus loading capacitances.
[6] $\overline{RDY}$ returns high after a read of the ADC. In single conversion mode and continuous conversion mode, the same data can be read again, if required, while $\overline{RDY}$ is high, although care should be taken to ensure that subsequent reads do not occur close to the next output update. In continuous read mode, the digital word can be read only once.

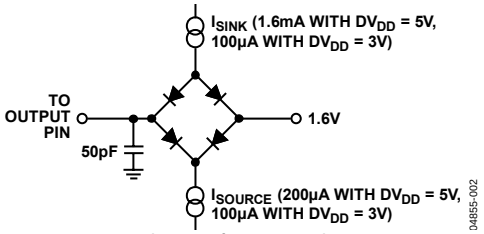
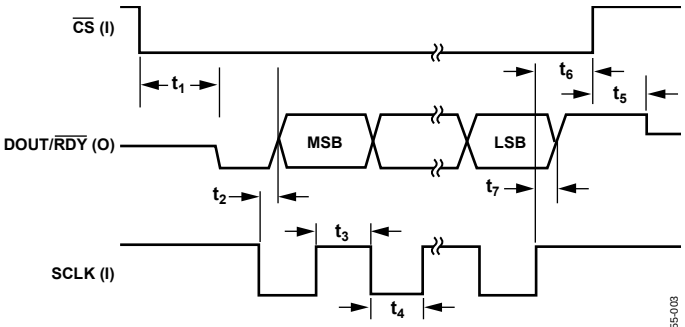


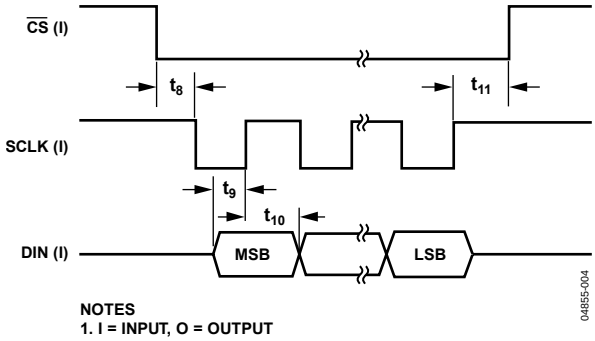
Figure 2. Load Circuit for Timing Characterization

TIMING DIAGRAMS



NOTES
1. I = INPUT, O = OUTPUT

Figure 3. Read Cycle Timing Diagram



NOTES
1. I = INPUT, O = OUTPUT

Figure 4. Write Cycle Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Ratings
AV_{DD} to GND	−0.3 V to +7 V
DV_{DD} to GND	−0.3 V to +7 V
Analog Input Voltage to GND	−0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to GND	−0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to GND	−0.3 V to DV_{DD} + 0.3 V
AIN/Digital Input Current	10 mA
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
TSSOP	
θ_{JA} Thermal Impedance	128°C/W
θ_{JC} Thermal Impedance	14°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

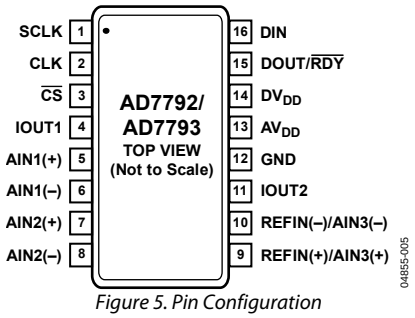


Figure 5. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SCLK	Serial Clock Input. This serial clock input is for data transfers to and from the ADC. The SCLK has a Schmitt-triggered input, making the interface suitable for opto-isolated applications. The serial clock can be continuous with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to or from the ADC in smaller batches of data.
2	CLK	Clock In/Clock Out. The internal clock can be made available at this pin. Alternatively, the internal clock can be disabled, and the ADC can be driven by an external clock. This allows several ADCs to be driven from a common clock, allowing simultaneous conversions to be performed.
3	$\overline{CS}$	Chip Select Input. This is an active low logic input used to select the ADC. $\overline{CS}$ can be used to select the ADC in systems with more than one device on the serial bus or as a frame synchronization signal in communicating with the device. $\overline{CS}$ can be hardwired low, allowing the ADC to operate in 3-wire mode with SCLK, DIN, and DOUT used to interface with the device.
4	IOUT1	Output of Internal Excitation Current Source. The internal excitation current source can be made available at this pin. The excitation current source is programmable so that the current can be 10 µA, 210 µA, or 1 mA. Either IEXC1 or IEXC2 can be switched to this output.
5	AIN1(+)	Analog Input. AIN1(+) is the positive terminal of the differential analog input pair AIN1(+)/AIN1(–).
6	AIN1(–)	Analog Input. AIN1(–) is the negative terminal of the differential analog input pair AIN1(+)/AIN1(–).
7	AIN2(+)	Analog Input. AIN2(+) is the positive terminal of the differential analog input pair AIN2(+)/AIN2(–).
8	AIN2(–)	Analog Input. AIN2(–) is the negative terminal of the differential analog input pair AIN2(+)/AIN2(–).
9	REFIN(+)/AIN3(+)	Positive Reference Input/Analog Input. An external reference can be applied between REFIN(+) and REFIN(–). REFIN(+) can lie anywhere between AV_{DD} and GND + 0.1 V. The nominal reference voltage REFIN(+) − REFIN(–) is 2.5 V, but the part functions with a reference from 0.1 V to AV_{DD}. Alternatively, this pin can function as AIN3(+) where AIN3(+) is the positive terminal of the differential analog input pair AIN3(+)/AIN3(–).
10	REFIN(–)/AIN3(–)	Negative Reference Input/Analog Input. REFIN(–) is the negative reference input for REFIN. This reference input can lie anywhere between GND and AV_{DD} − 0.1 V. This pin also functions as AIN3(–), which is the negative terminal of the differential analog input pair AIN3(+)/AIN3(–).
11	IOUT2	Output of Internal Excitation Current Source. The internal excitation current source can be made available at this pin. The excitation current source is programmable so that the current can be 10 µA, 210 µA, or 1 mA. Either IEXC1 or IEXC2 can be switched to this output.
12	GND	Ground Reference Point.
13	AV_{DD}	Supply Voltage, 2.7 V to 5.25 V.
14	DV_{DD}	Digital Interface Supply Voltage. The logic levels for the serial interface pins are related to this supply, which is between 2.7 V and 5.25 V. The DV_{DD} voltage is independent of the voltage on AV_{DD}; therefore, AV_{DD} can equal 5 V with DV_{DD} at 3 V or vice versa.

Pin No.	Mnemonic	Description
15	DOUT/$\overline{\text{RDY}}$	Serial Data Output/Data Ready Output. DOUT/$\overline{\text{RDY}}$ serves a dual purpose. It functions as a serial data output pin to access the output shift register of the ADC. The output shift register can contain data from any of the on-chip data or control registers. In addition, DOUT/$\overline{\text{RDY}}$ operates as a data ready pin, going low to indicate the completion of a conversion. If the data is not read after the conversion, the pin goes high before the next update occurs. The DOUT/$\overline{\text{RDY}}$ falling edge can be used as an interrupt to a processor, indicating that valid data is available. With an external serial clock, the data can be read using the DOUT/$\overline{\text{RDY}}$ pin. With $\overline{\text{CS}}$ low, the data/control word information is placed on the DOUT/$\overline{\text{RDY}}$ pin on the SCLK falling edge and is valid on the SCLK rising edge.
16	DIN	Serial Data Input. This serial data input is to the input shift register on the ADC. Data in this shift register is transferred to the control registers within the ADC; the register selection bits of the communications register identify the appropriate register.

OUTPUT NOISE AND RESOLUTION SPECIFICATIONS

EXTERNAL REFERENCE

Table 5 shows the output rms noise of the AD7792/AD7793 for some of the update rates and gain settings. The numbers given are for the bipolar input range with an external 2.5 V reference. These numbers are typical and are generated with a differential input voltage of 0 V. Table 6 and Table 7 show the effective resolution, with the output peak-to-peak (p-p) resolution shown in parentheses for the AD7793 and AD7792, respectively. It is important to note that the effective resolution is calculated using the rms noise, while the p-p resolution is based on the p-p noise. The p-p resolution represents the resolution for which there is no code flicker. These numbers are typical and are rounded to the nearest LSB.

Table 5. Output RMS Noise (μV) vs. Gain and Output Update Rate for the AD7792 and AD7793 Using an External 2.5 V Reference

Update Rate (Hz)	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
4.17	0.64	0.6	0.29	0.22	0.1	0.065	0.039	0.041
8.33	1.04	0.96	0.38	0.26	0.13	0.078	0.057	0.055
16.7	1.55	1.45	0.54	0.36	0.18	0.11	0.087	0.086
33.2	2.3	2.13	0.74	0.5	0.23	0.17	0.124	0.118
62	2.95	2.85	0.92	0.58	0.29	0.2	0.153	0.144
123	4.89	4.74	1.49	1	0.48	0.32	0.265	0.283
242	11.76	9.5	4.02	1.96	0.88	0.45	0.379	0.397
470	11.33	9.44	3.07	1.79	0.99	0.63	0.568	0.593

Table 6. Typical Resolution (Bits) vs. Gain and Output Update Rate for the AD7793 Using an External 2.5 V Reference

Update Rate (Hz)	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
4.17	23 (20.5)	22 (19.5)	22 (19.5)	21.5 (19)	21.5 (19)	21 (18.5)	21 (18.5)	20 (17.5)
8.33	22 (19.5)	21.5 (19)	21.5 (19)	21 (18.5)	21 (18.5)	21 (18.5)	20.5 (18)	19.5 (17)
16.7	21.5 (19)	20.5 (18)	21 (18.5)	20.5 (18)	20.5 (18)	20.5 (18)	20 (17.5)	19 (16.5)
33.2	21 (18.5)	20 (17.5)	20.5 (18)	20 (17.5)	20.5 (18)	20 (17.5)	19 (16.5)	18.5 (16)
62	20.5 (18)	19.5 (17)	20.5 (18)	20 (17.5)	20 (17.5)	19.5 (17)	19 (16.5)	18 (15.5)
123	20 (17.5)	19 (16.5)	19.5 (17)	19 (16.5)	19.5 (17)	19 (16.5)	18 (15.5)	17 (14.5)
242	18.5 (16)	18 (15.5)	18 (15.5)	18 (15.5)	18.5 (16)	18.5 (16)	17.5 (15)	16.5 (14)
470	18.5 (16)	18 (15.5)	18.5 (16)	18.5 (16)	18 (15.5)	18 (15.5)	17 (14.5)	16 (13.5)

Table 7. Typical Resolution (Bits) vs. Gain and Output Update Rate for the AD7792 Using an External 2.5 V Reference

Update Rate (Hz)	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
4.17	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
8.33	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
16.7	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
33.2	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
62	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.5)
123	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	165 (15.5)	16 (14.5)
242	16 (16)	16 (15.5)	16 (15.5)	16 (15.5)	16 (16)	16 (16)	16 (15)	16 (14)
470	16 (16)	16 (15.5)	16 (16)	16 (16)	16 (15.5)	16 (15.5)	16 (14.5)	15.5 (13.5)

INTERNAL REFERENCE

Table 8 shows the output rms noise of the AD7792/AD7793 for some of the update rates and gain settings. The numbers given are for the bipolar input range with the internal 1.17 V reference. These numbers are typical and are generated with a differential input voltage of 0 V. Table 9 and Table 10 show the effective resolution, with the output peak-to-peak (p-p) resolution given in parentheses for the AD7793 and AD7792, respectively. It is important to note that the effective resolution is calculated using the rms noise, while the p-p resolution is calculated based on p-p noise. The p-p resolution represents the resolution for which there is no code flicker. These numbers are typical and are rounded to the nearest LSB.

Table 8. Output RMS Noise (μV) vs. Gain and Output Update Rate for the AD7792 and AD7793 Using the Internal Reference

Update Rate (Hz)	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
4.17	0.81	0.67	0.32	0.2	0.13	0.065	0.04	0.039
8.33	1.18	1.11	0.41	0.25	0.16	0.078	0.058	0.059
16.7	1.96	1.72	0.55	0.36	0.25	0.11	0.088	0.088
33.2	2.99	2.48	0.83	0.48	0.33	0.17	0.13	0.12
62	3.6	3.25	1.03	0.65	0.46	0.2	0.15	0.15
123	5.83	5.01	1.69	0.96	0.67	0.32	0.25	0.26
242	11.22	8.64	2.69	1.9	1.04	0.45	0.35	0.34
470	12.46	10.58	4.58	2	1.27	0.63	0.50	0.49

Table 9. Typical Resolution (Bits) vs. Gain and Output Update Rate for the AD7793 Using the Internal Reference

Update Rate (Hz)	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
4.17	21.5 (19)	20.5 (18)	21 (18.5)	20.5 (18)	20 (17.5)	20 (17.5)	20 (17.5)	19 (16.5)
8.33	21 (18.5)	20 (17.5)	20.5 (18)	20 (17.5)	20 (17.5)	20 (17.5)	19 (16.5)	18 (15.5)
16.7	20 (17.5)	19.5 (17)	20 (17.5)	19.5 (17)	19 (16.5)	19.5 (17)	18.5 (16)	17.5 (15)
33.2	19.5 (17)	19 (16.5)	19.5 (17)	19 (16.5)	19 (16.5)	18.5 (16)	18 (15.5)	17 (14.5)
62	19.5 (17)	18.5 (16)	19 (16.5)	19 (16.5)	18.5 (16)	18.5 (16)	18 (15.5)	17 (14.5)
123	18.5 (16)	18 (15.5)	18.5 (16)	18 (15.5)	17.5 (15)	18 (15.5)	17 (14.5)	16 (13.5)
242	17.5 (15)	17 (14.5)	17.5 (15)	17 (14.5)	17 (14.5)	17.5 (15)	16.5 (14)	15.5 (13)
470	17.5 (15)	17 (14.5)	17 (14.5)	17 (14.5)	17 (14.5)	17 (14.5)	16 (13.5)	15 (12.5)

Table 10. Typical Resolution (Bits) vs. Gain and Output Update Rate for the AD7792 Using the Internal Reference

Update Rate (Hz)	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
4.17	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
8.33	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.5)
16.7	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15)
33.2	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.5)	16 (14.5)
62	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.5)	16 (14.5)
123	16 (16)	16 (15.5)	16 (16)	16 (15.5)	16 (15)	16 (15.5)	16 (14.5)	15.5 (13.5)
242	16 (15)	16 (14.5)	16 (15)	16 (14.5)	16 (14.5)	16 (15)	16 (14)	15 (13)
470	16 (15)	16 (14.5)	16 (14.5)	16 (14.5)	16 (14.5)	16 (14.5)	15.5 (13.5)	14.5 (12.5)

TYPICAL PERFORMANCE CHARACTERISTICS

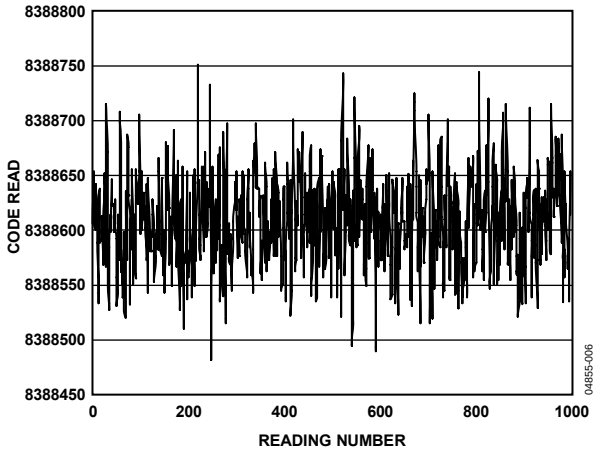


Figure 6. Typical Noise Plot (Internal Reference, Gain = 64, Update Rate = 16.7 Hz) for AD7793

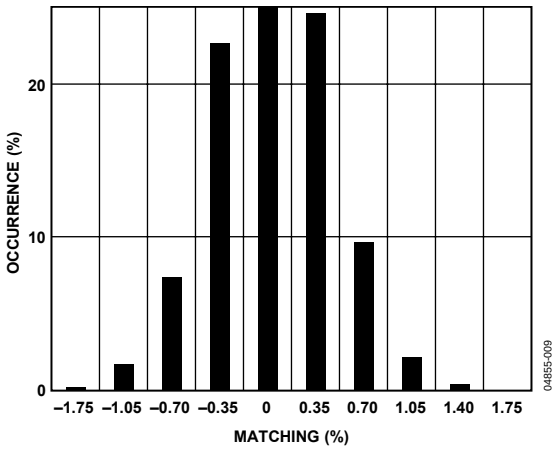


Figure 9. Excitation Current Matching (1 mA) at Ambient Temperature

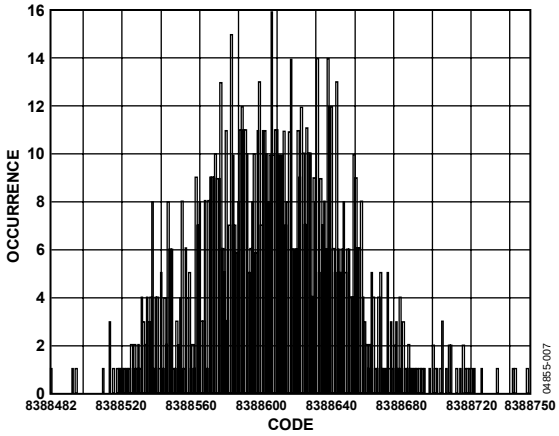


Figure 7. Noise Distribution Histogram for AD7793 (Internal Reference, Gain = 64, Update Rate = 16.7 Hz)

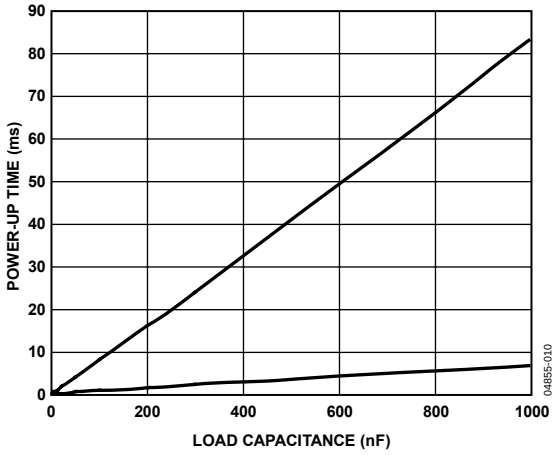


Figure 10. Bias Voltage Generator Power-Up Time vs. Load Capacitance

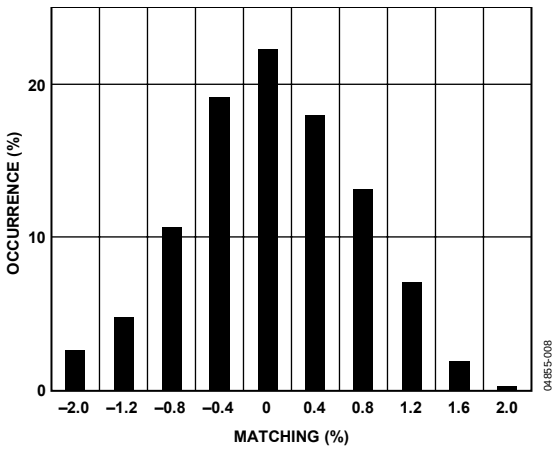


Figure 8. Excitation Current Matching (210 µA) at Ambient Temperature

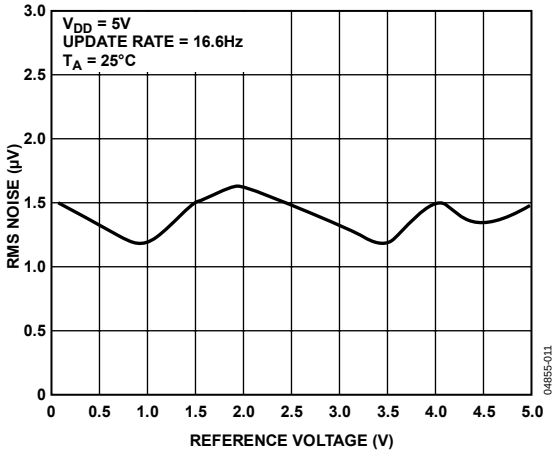


Figure 11. RMS Noise vs. Reference Voltage (Gain = 1)

ON-CHIP REGISTERS

The ADC is controlled and configured via a number of on-chip registers, which are described on the following pages. In the following descriptions, *set* implies a Logic 1 state and *cleared* implies a Logic 0 state, unless otherwise stated.

COMMUNICATIONS REGISTER

RS2, RS1, RS0 = 0, 0, 0

The communications register is an 8-bit write-only register. All communications to the part must start with a write operation to the communications register. The data written to the communications register determines whether the next operation is a read or write operation, and to which register this operation takes place. For read or write operations, once the subsequent read or write operation to the selected register is complete, the interface returns to where it expects a write operation to the communications register. This is the default state of the interface and, on power-up or after a reset, the ADC is in this default state waiting for a write operation to the communications register. In situations where the interface sequence is lost, a write operation of at least 32 serial clock cycles with DIN high returns the ADC to this default state by resetting the entire part. Table 11 outlines the bit designations for the communications register. CR0 through CR7 indicate the bit location, CR denoting the bits are in the communications register. CR7 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
$\overline{\text{WEN}}$(0)	R/$\overline{\text{W}}$(0)	RS2(0)	RS1(0)	RS0(0)	CREAD(0)	0(0)	0(0)

Table 11. Communications Register Bit Designations

Bit Location	Bit Name	Description
CR7	$\overline{\text{WEN}}$	Write Enable Bit. A 0 must be written to this bit so that the write to the communications register actually occurs. If a 1 is the first bit written, the part does not clock on to subsequent bits in the register. It stays at this bit location until a 0 is written to this bit. Once a 0 is written to the $\overline{\text{WEN}}$ bit, the next seven bits are loaded to the communications register.
CR6	R/$\overline{\text{W}}$	A 0 in this bit location indicates that the next operation is a write to a specified register. A 1 in this position indicates that the next operation is a read from the designated register.
CR5 to CR3	RS2 to RS0	Register Address Bits. These address bits are used to select which of the ADC's registers are being selected during this serial interface communication. See Table 12.
CR2	CREAD	Continuous Read of the Data Register. When this bit is set to 1 (and the data register is selected), the serial interface is configured so that the data register can be continuously read. For example, the contents of the data register are placed on the DOUT pin automatically when the SCLK pulses are applied after the $\overline{\text{RDY}}$ pin goes low to indicate that a conversion is complete. The communications register does not have to be written to for data reads. To enable continuous read mode, the instruction 01011100 must be written to the communications register. To exit the continuous read mode, the instruction 01011000 must be written to the communications register while the $\overline{\text{RDY}}$ pin is low. While in continuous read mode, the ADC monitors activity on the DIN line so that it can receive the instruction to exit continuous read mode. Additionally, a reset occurs if 32 consecutive 1s are seen on DIN. Therefore, DIN should be held low in continuous read mode until an instruction is to be written to the device.
CR1 to CR0	0	These bits must be programmed to Logic 0 for correct operation.

Table 12. Register Selection

RS2	RS1	RS0	Register	Register Size
0	0	0	Communications Register During a Write Operation	8-bit
0	0	0	Status Register During a Read Operation	8-bit
0	0	1	Mode Register	16-bit
0	1	0	Configuration Register	16-bit
0	1	1	Data Register	16-/24-bit
1	0	0	ID Register	8-bit
1	0	1	IO Register	8-bit
1	1	0	Offset Register	16-bit (AD7792)/24-bit (AD7793)
1	1	1	Full-Scale Register	16-bit (AD7792)/24-bit (AD7793)

STATUS REGISTER

RS2, RS1, RS0 = 0, 0, 0; Power-On/Reset = 0x80 (AD7792)/0x88 (AD7793)

The status register is an 8-bit read-only register. To access the ADC status register, the user must write to the communications register, select the next operation to be a read, and load Bit RS2, Bit RS1, and Bit RS0 with 0. Table 13 outlines the bit designations for the status register. SR0 through SR7 indicate the bit locations, and SR denotes that the bits are in the status register. SR7 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
$\overline{\text{RDY}}$(1)	ERR(0)	0(0)	0(0)	0/1	CH2(0)	CH1(0)	CH0(0)

Table 13. Status Register Bit Designations

Bit Location	Bit Name	Description
SR7	$\overline{\text{RDY}}$	Ready Bit for ADC. Cleared when data is written to the ADC data register. The $\overline{\text{RDY}}$ bit is set automatically after the ADC data register has been read or a period of time before the data register is updated with a new conversion result to indicate to the user not to read the conversion data. It is also set when the part is placed in power-down mode. The end of a conversion is indicated by the DOUT/$\overline{\text{RDY}}$ pin also. This pin can be used as an alternative to the status register for monitoring the ADC for conversion data.
SR6	ERR	ADC Error Bit. This bit is written to at the same time as the $\overline{\text{RDY}}$ bit. Set to indicate that the result written to the ADC data register has been clamped to all 0s or all 1s. Error sources include overrange and underrange. Cleared by a write operation to start a conversion.
SR5 to SR4	0	These bits are automatically cleared.
SR3	0/1	This bit is automatically cleared on the AD7792 and is automatically set on the AD7793.
SR2 to SR0	CH2 to CH0	These bits indicate which channel is being converted by the ADC.

MODE REGISTER

RS2, RS1, RS0 = 0, 0, 1; Power-On/Reset = 0x000A

The mode register is a 16-bit register from which data can be read or to which data can be written. This register is used to select the operating mode, update rate, and clock source. Table 14 outlines the bit designations for the mode register. MR0 through MR15 indicate the bit locations, MR denoting the bits are in the mode register. MR15 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit. Any write to the setup register resets the modulator and filter and sets the $\overline{\text{RDY}}$ bit.

MR15	MR14	MR13	MR12	MR11	MR10	MR9	MR8
MD2(0)	MD1(0)	MD0(0)	0(0)	0(0)	0(0)	0(0)	0(0)
MR7	**MR6**	**MR5**	**MR4**	**MR3**	**MR2**	**MR1**	**MR0**
CLK1(0)	CLK0(0)	0(0)	0(0)	FS3(1)	FS2(0)	FS1(1)	FS0(0)

Table 14. Mode Register Bit Designations

Bit Location	Bit Name	Description		
MR15 to MR13	MD2 to MD0	Mode Select Bits. These bits select the operational mode of the AD7792/AD7793 (see Table 15).		
MR12 to MR8	0	These bits must be programmed with a Logic 0 for correct operation.		
MR7 to MR6	CLK1 to CLK0	These bits are used to select the clock source for the AD7792/AD7793. Either an on-chip 64 kHz clock can be used, or an external clock can be used. The ability to override using an external clock allows several AD7792/AD7793 devices to be synchronized. In addition, 50 Hz/60 Hz is improved when an accurate external clock drives the AD7792/AD7793.		
		CLK1	**CLK0**	**ADC Clock Source**
		0	0	Internal 64 kHz Clock. Internal clock is not available at the CLK pin.
		0	1	Internal 64 kHz Clock. This clock is made available at the CLK pin.
		1	0	External 64 kHz Clock Used. An external clock gives better 50 Hz/60 Hz rejection. See specifications for external clock.
		1	1	External Clock Used. The external clock is divided by 2 within the AD7792/AD7793.
MR5 to MR4	0	These bits must be programmed with a Logic 0 for correct operation.		
MR3 to MR0	FS3 to FS0	Filter Update Rate Select Bits (see Table 16).		

Table 15. Operating Modes

MD2	MD1	MD0	Mode
0	0	0	Continuous Conversion Mode (Default). In continuous conversion mode, the ADC continuously performs conversions and places the result in the data register. RDY goes low when a conversion is complete. The user can read these conversions by placing the device in continuous read mode, whereby the conversions are automatically placed on the DOUT line when SCLK pulses are applied. Alternatively, the user can instruct the ADC to output the conversion by writing to the communications register. After power-on, a channel change, or a write to the mode, configuration, or IO registers, the first conversion is available after a period of $2/f_{ADC}$. Subsequent conversions are available at a frequency of f_{ADC}.
0	0	1	Single Conversion Mode. When single conversion mode is selected, the ADC powers up and performs a single conversion. The oscillator requires 1 ms to power up and settle. The ADC then performs the conversion, which takes a time of $2/f_{ADC}$. The conversion result is placed in the data register, RDY goes low, and the ADC returns to power-down mode. The conversion remains in the data register, and RDY remains active low until the data is read or another conversion is performed.
0	1	0	Idle Mode. In idle mode, the ADC filter and modulator are held in a reset state, although the modulator clocks are still provided.
0	1	1	Power-Down Mode. In power-down mode, all the AD7792/AD7793 circuitry is powered down, including the current sources, burnout currents, bias voltage generator, and CLKOUT circuitry.
1	0	0	Internal Zero-Scale Calibration. An internal short is automatically connected to the enabled channel. A calibration takes 2 conversion cycles to complete. RDY goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured offset coefficient is placed in the offset register of the selected channel.
1	0	1	Internal Full-Scale Calibration. A full-scale input voltage is automatically connected to the selected analog input for this calibration. When the gain equals 1, a calibration takes 2 conversion cycles to complete. For higher gains, 4 conversion cycles are required to perform the full-scale calibration. RDY goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured full-scale coefficient is placed in the full-scale register of the selected channel. Internal full-scale calibrations cannot be performed when the gain equals 128. With this gain setting, a system full-scale calibration can be performed. A full-scale calibration is required each time the gain of a channel is changed to minimize the full-scale error.
1	1	0	System Zero-Scale Calibration. User should connect the system zero-scale input to the channel input pins as selected by the CH2 to CH0 bits. A system offset calibration takes 2 conversion cycles to complete. RDY goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured offset coefficient is placed in the offset register of the selected channel.
1	1	1	System Full-Scale Calibration. User should connect the system full-scale input to the channel input pins as selected by the CH2 to CH0 bits. A calibration takes 2 conversion cycles to complete. RDY goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured full-scale coefficient is placed in the full-scale register of the selected channel. A full-scale calibration is required each time the gain of a channel is changed.

Table 16. Update Rates Available

FS3	FS2	FS1	FS0	f_{ADC} (Hz)	t_{SETTLE} (ms)	Rejection @ 50 Hz/60 Hz (Internal Clock)
0	0	0	0	x	x	
0	0	0	1	470	4	
0	0	1	0	242	8	
0	0	1	1	123	16	
0	1	0	0	62	32	
0	1	0	1	50	40	
0	1	1	0	39	48	
0	1	1	1	33.2	60	
1	0	0	0	19.6	101	90 dB (60 Hz only)

FS3	FS2	FS1	FS0	f_{ADC} (Hz)	t_{SETTLE} (ms)	Rejection @ 50 Hz/60 Hz (Internal Clock)
1	0	0	1	16.7	120	80 dB (50 Hz only)
1	0	1	0	16.7	120	65 dB (50 Hz and 60 Hz)
1	0	1	1	12.5	160	66 dB (50 Hz and 60 Hz)
1	1	0	0	10	200	69 dB (50 Hz and 60 Hz)
1	1	0	1	8.33	240	70 dB (50 Hz and 60 Hz)
1	1	1	0	6.25	320	72 dB (50 Hz and 60 Hz)
1	1	1	1	4.17	480	74 dB (50 Hz and 60 Hz)

CONFIGURATION REGISTER

RS2, RS1, RS0 = 0, 1, 0; Power-On/Reset = 0x0710

The configuration register is a 16-bit register from which data can be read or to which data can be written. This register is used to configure the ADC for unipolar or bipolar mode, enable or disable the buffer, enable or disable the burnout currents, select the gain, and select the analog input channel. Table 17 outlines the bit designations for the filter register. CON0 through CON15 indicate the bit locations; CON denotes that the bits are in the configuration register. CON15 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

CON15	CON14	CON13	CON12	CON11	CON10	CON9	CON8
VBIAS1(0)	VBIAS0(0)	BO(0)	U/$\overline{B}$(0)	BOOST(0)	G2(1)	G1(1)	G0(1)
CON7	**CON6**	**CON5**	**CON4**	**CON3**	**CON2**	**CON1**	**CON0**
REFSEL(0)	0(0)	0(0)	BUF(1)	0(0)	CH2(0)	CH1(0)	CH0(0)

Table 17. Configuration Register Bit Designations

Bit Location	Bit Name	Description				
CON15 to CON14	VBIAS1 to VBIAS0	Bias Voltage Generator Enable. The negative terminal of the analog inputs can be biased up to $AV_{DD}/2$. These bits are used in conjunction with the boost bit.				
		VBIAS1	**VBIAS0**		**Bias Voltage**	
		0	0		Bias voltage generator disabled	
		0	1		Bias voltage connected to AIN1(–)	
		1	0		Bias voltage connected to AIN2(–)	
		1	1		Reserved	
CON13	BO	Burnout Current Enable Bit. When this bit is set to 1 by the user, the 100 nA current sources in the signal path are enabled. When BO = 0, the burnout currents are disabled. The burnout currents can be enabled only when the buffer or in-amp is active.				
CON12	U/$\overline{B}$	Unipolar/Bipolar Bit. Set by user to enable unipolar coding; that is, zero differential input results in 0x000000 output, and a full-scale differential input results in 0xFFFFFF output. Cleared by the user to enable bipolar coding. Negative full-scale differential input results in an output code of 0x000000, zero differential input results in an output code of 0x800000, and a positive full-scale differential input results in an output code of 0xFFFFFF.				
CON11	BOOST	This bit is used in conjunction with the VBIAS1 and VBIAS0 bits. When set, the current consumed by the bias voltage generator is increased. This reduces its power-up time.				
CON10 to CON8	G2 to G0	Gain Select Bits. Written by the user to select the ADC input range as follows:				
		G2	**G1**	**G0**	**Gain**	**ADC Input Range (2.5 V Reference)**
		0	0	0	1 (In-amp not used)	2.5 V
		0	0	1	2 (In-amp not used)	1.25 V
		0	1	0	4	625 mV
		0	1	1	8	312.5 mV
		1	0	0	16	156.2 mV
		1	0	1	32	78.125 mV
		1	1	0	64	39.06 mV
		1	1	1	128	19.53 mV

Bit Location	Bit Name	Description				
CON7	REFSEL	Reference Select Bit. The reference source for the ADC is selected using this bit.				
		REFSEL	**Reference Source**			
		0	External Reference Applied between REFIN(+) and REFIN(–).			
		1	Internal Reference Selected.			
CON6 to CON5	0	These bits must be programmed with a Logic 0 for correct operation.				
CON4	BUF	Configures the ADC for buffered or unbuffered mode of operation. If *cleared*, the ADC operates in unbuffered mode, lowering the power consumption of the device. If *set*, the ADC operates in buffered mode, allowing the user to place source impedances on the front end without contributing gain errors to the system. The buffer can be disabled when the gain equals 1 or 2. For higher gains, the buffer is automatically enabled. With the buffer disabled, the voltage on the analog input pins can be from 30 mV below GND to 30 mV above AV_{DD}. When the buffer is enabled, it requires some headroom, so the voltage on any input pin must be limited to 100 mV within the power supply rails.				
CON3	0	This bit must be programmed with a Logic 0 for correct operation.				
CON2 to CON0	CH2 to CH0	Channel Select Bits. Written by the user to select the active analog input channel to the ADC.				
		CH2	**CH1**	**CH0**	**Channel**	**Calibration Pair**
		0	0	0	AIN1(+) – AIN1(–)	0
		0	0	1	AIN2(+) – AIN2(–)	1
		0	1	0	AIN3(+) – AIN3(–)	2
		0	1	1	AIN1(–) – AIN1(–)	0
		1	0	0	Reserved	
		1	0	1	Reserved	
		1	1	0	Temp Sensor	Automatically selects gain = 1 and internal reference
		1	1	1	AV_{DD} Monitor	Automatically selects gain = 1/6 and 1.17 V reference

DATA REGISTER

RS2, RS1, RS0 = 0, 1, 1; Power-On/Reset = 0x0000(00)

The conversion result from the ADC is stored in this data register. This is a read-only register. On completion of a read operation from this register, the $\overline{RDY}$ bit/pin is set.

ID REGISTER

RS2, RS1, RS0 = 1, 0, 0; Power-On/Reset = 0xXA (AD7792)/0xXB (AD7793)

The identification number for the AD7792/AD7793 is stored in the ID register. This is a read-only register.

IO REGISTER

RS2, RS1, RS0 = 1, 0, 1; Power-On/Reset = 0x00

The IO register is an 8-bit register from which data can be read or to which data can be written. This register is used to enable and select the value of the excitation currents. Table 18 outlines the bit designations for the IO register. IO0 through IO7 indicate the bit locations; IO denotes that the bits are in the IO register. IO7 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
0(0)	0(0)	0(0)	0(0)	IEXCDIR1(0)	IEXCDIR0(0)	IEXCEN1(0)	IEXCEN0(0)

Table 18. IO Register Bit Designations

Bit Location	Bit Name	Description		
IO7 to IO4	0	These bits must be programmed with a Logic 0 for correct operation.		
IO3 to IO2	IEXCDIR1 to IEXCDIR0	Direction of current sources select bits.		
		IEXCDIR1	**IEXCDIR0**	**Current Source Direction**
		0	0	Current Source IEXC1 connected to Pin IOUT1, Current Source IEXC2 connected to Pin IOUT2.
		0	1	Current Source IEXC1 connected to Pin IOUT2, Current Source IEXC2 connected to Pin IOUT1.
		1	0	Both current sources connected to Pin IOUT1. Permitted when the current sources are set to 10 μA or 210 μA only.
		1	1	Both current sources connected to Pin IOUT2. Permitted when the current sources are set to 10 μA or 210 μA only.
IO1 to IO0	IEXCEN1 to IEXCEN0	These bits are used to enable and disable the current sources along with selecting the value of the excitation currents.		
		IEXCEN1	**IEXCEN0**	**Current Source Value**
		0	0	Excitation Current Disabled.
		0	1	10 μA
		1	0	210 μA
		1	1	1 mA

OFFSET REGISTER

RS2, RS1, RS0 = 1, 1, 0; Power-On/Reset = 0x8000 (AD7792)/0x800000 (AD7793)

Each analog input channel has a dedicated offset register that holds the offset calibration coefficient for the channel. This register is 16 bits wide on the AD7792 and 24 bits wide on the AD7793, and its power-on/reset value is 0x8000(00). The offset register is used in conjunction with its associated full-scale register to form a register pair. The power-on-reset value is automatically overwritten if an internal or system zero-scale calibration is initiated by the user. The offset register is a read/write register. However, the AD7792/AD7793 must be in idle mode or power-down mode when writing to the offset register.

FULL-SCALE REGISTER

RS2, RS1, RS0 = 1, 1, 1; Power-On/Reset = 0x5XXX (AD7792)/0x5XXX00 (AD7793)

The full-scale register is a 16-bit register on the AD7792 and a 24-bit register on the AD7793. The full-scale register holds the full-scale calibration coefficient for the ADC. The AD7792/AD7793 have 3 full-scale registers, each channel having a dedicated full-scale register. The full-scale registers are read/write registers; however, when writing to the full-scale registers, the ADC must be placed in power-down mode or idle mode. These registers are configured on power-on with factory-calibrated full-scale calibration coefficients, the calibration being performed at gain = 1. Therefore, every device has different default coefficients. The coefficients are different depending on whether the internal reference or an external reference is selected. The default value is automatically overwritten if an internal or system full-scale calibration is initiated by the user, or the full-scale register is written to.

ADC CIRCUIT INFORMATION

OVERVIEW

The AD7792/AD7793 are low power ADCs that incorporate a Σ-Δ modulator, a buffer, reference, in-amp, and an on-chip digital filter intended for the measurement of wide dynamic range, low frequency signals such as those in pressure transducers, weigh scales, and temperature measurement applications.

The part has three differential inputs that can be buffered or unbuffered. The device can be operated with the internal 1.17 V reference, or an external reference can be used. Figure 12 shows the basic connections required to operate the part.

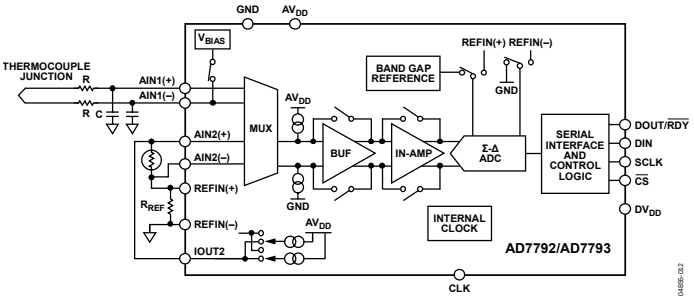


Figure 12. Basic Connection Diagram

The output rate of the AD7792/AD7793 (f_{ADC}) is user-programmable. The allowable update rates, along with their corresponding settling times, are listed in Table 16. Normal mode rejection is the major function of the digital filter. Simultaneous 50 Hz and 60 Hz rejection is optimized when the update rate equals 16.7 Hz or less as notches are placed at both 50 Hz and 60 Hz with these update rates. See Figure 14.

The AD7792/AD7793 use slightly different filter types, depending on the output update rate so that the rejection of quantization noise and device noise is optimized. When the update rate is from 4.17 Hz to 12.5 Hz, a Sinc3 filter, along with an averaging filter, is used. When the update rate is from 16.7 Hz to 39 Hz, a modified Sinc3 filter is used. This filter provides simultaneous 50 Hz/60 Hz rejection when the update rate equals 16.7 Hz. A Sinc4 filter is used when the update rate is from 50 Hz to 242 Hz. Finally, an integrate-only filter is used when the update rate equals 470 Hz.

Figure 13 to Figure 16 show the frequency response of the different filter types for several update rates.

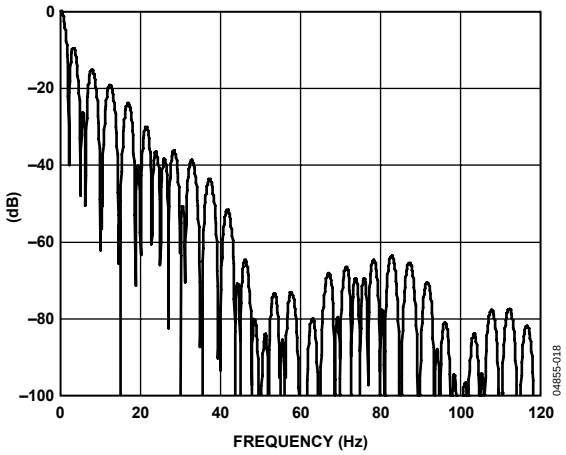


Figure 13. Filter Profile with Update Rate = 4.17 Hz

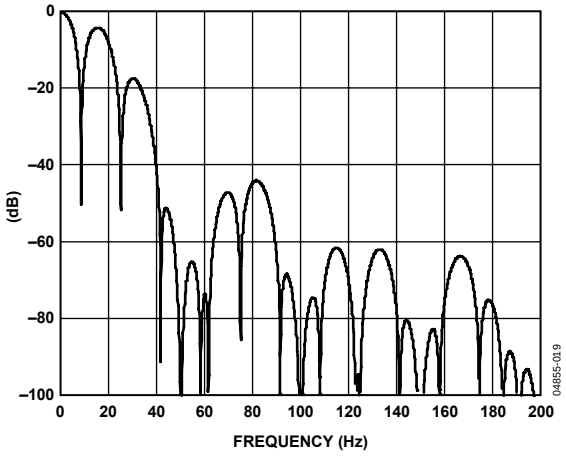


Figure 14. Filter Profile with Update Rate = 16.7 Hz

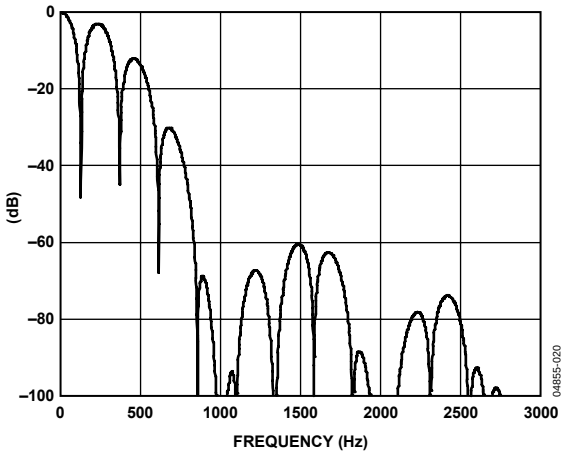


Figure 15. Filter Profile with Update Rate = 242 Hz

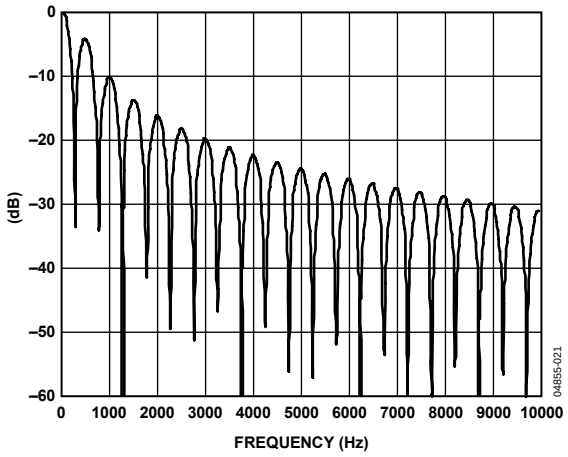


Figure 16. Filter Response at 470 Hz Update Rate

DIGITAL INTERFACE

The programmable functions of the AD7792/AD7793 are controlled using a set of on-chip registers. Data is written to these registers via the serial interface of the device; read access to the on-chip registers is also provided by this interface. All communications with the device must start with a write to the communications register. After power-on or reset, the device expects a write to its communications register. The data written to this register determines whether the next operation is a read operation or a write operation and determines to which register this read or write operation occurs. Therefore, write access to any of the other registers on the part begins with a write operation to the communications register followed by a write to the selected register. A read operation from any other register (except when continuous read mode is selected) starts with a write to the communications register followed by a read operation from the selected register.

The serial interfaces of the AD7792/AD7793 consist of four signals: $\overline{CS}$, DIN, SCLK, and DOUT/$\overline{RDY}$. The DIN line is used to transfer data into the on-chip registers, and DOUT/$\overline{RDY}$ is used for accessing from the on-chip registers. SCLK is the serial clock input for the device, and all data transfers (either on DIN or DOUT/$\overline{RDY}$) occur with respect to the SCLK signal. The DOUT/$\overline{RDY}$ pin operates as a data-ready signal also, the line going low when a new data-word is available in the output register. It is reset high when a read operation from the data register is complete. It also goes high prior to the updating of the data register to indicate when not to read from the device, to ensure that a data read is not attempted while the register is being updated. $\overline{CS}$ is used to select a device. It can be used to decode the AD7792/AD7793 in systems where several components are connected to the serial bus.

Figure 3 and Figure 4 show timing diagrams for interfacing to the AD7792/AD7793 with $\overline{CS}$ being used to decode the part. Figure 3 shows the timing for a read operation from the AD7792/AD7793 output shift register, and Figure 4 shows the timing for a write operation to the input shift register. It is possible to read the same word from the data register several times, even though the DOUT/$\overline{RDY}$ line returns high after the first read operation. However, care must be taken to ensure that the read operations have been completed before the next output update occurs. In continuous read mode, the data register can be read only once.

The serial interface can operate in 3-wire mode by tying $\overline{CS}$ low. In this case, the SCLK, DIN, and DOUT/$\overline{RDY}$ lines are used to communicate with the AD7792/AD7793. The end of the conversion can be monitored using the $\overline{RDY}$ bit in the status register. This scheme is suitable for interfacing to microcontrollers. If $\overline{CS}$ is required as a decoding signal, it can be generated from a port pin. For microcontroller interfaces, it is recommended that SCLK idle high between data transfers.

The AD7792/AD7793 can be operated with $\overline{CS}$ being used as a frame synchronization signal. This scheme is useful for DSP interfaces. In this case, the first bit (MSB) is effectively clocked out by $\overline{CS}$, because $\overline{CS}$ would normally occur after the falling edge of SCLK in DSPs. The SCLK can continue to run between data transfers, provided the timing numbers are obeyed.

The serial interface can be reset by writing a series of 1s on the DIN input. If a Logic 1 is written to the AD7792/AD7793 line for at least 32 serial clock cycles, the serial interface is reset. This ensures that the interface can be reset to a known state if the interface gets lost due to a software error or some glitch in the system. Reset returns the interface to the state in which it is expecting a write to the communications register. This operation resets the contents of all registers to their power-on values. Following a reset, the user should allow a period of 500 μs before addressing the serial interface.

The AD7792/AD7793 can be configured to continuously convert or to perform a single conversion. See Figure 17 through Figure 19.

Single Conversion Mode

In single conversion mode, the AD7792/AD7793 are placed in shutdown mode between conversions. When a single conversion is initiated by setting MD2, MD1, MD0 to 0, 0, 1 in the mode register, the AD7792/AD7793 power up, perform a single conversion, and then return to shutdown mode. The on-chip oscillator requires 1 ms to power up. A conversion requires a time period of $2 \times t_{ADC}$. DOUT/$\overline{RDY}$ goes low to indicate the completion of a conversion. When the data-word has been read from the data register, DOUT/$\overline{RDY}$ goes high. If $\overline{CS}$ is low, DOUT/$\overline{RDY}$ remains high until another conversion is initiated and completed. The data register can be read several times, if required, even when DOUT/$\overline{RDY}$ has gone high.

Continuous Conversion Mode

This is the default power-up mode. The AD7792/AD7793 continuously converts, the $\overline{RDY}$ pin in the status register going low each time a conversion is completed. If $\overline{CS}$ is low, the DOUT/ $\overline{RDY}$ line also goes low when a conversion is complete. To read a conversion, the user writes to the communications register indicating that the next operation is a read of the data register. The digital conversion is placed on the DOUT/ $\overline{RDY}$ pin as soon as SCLK pulses are applied to the ADC. DOUT/$\overline{RDY}$ returns high when the conversion is read. The user can read this register additional times, if required. However, the user must ensure that the data register is not being accessed at the completion of the next conversion, otherwise the new conversion word is lost.

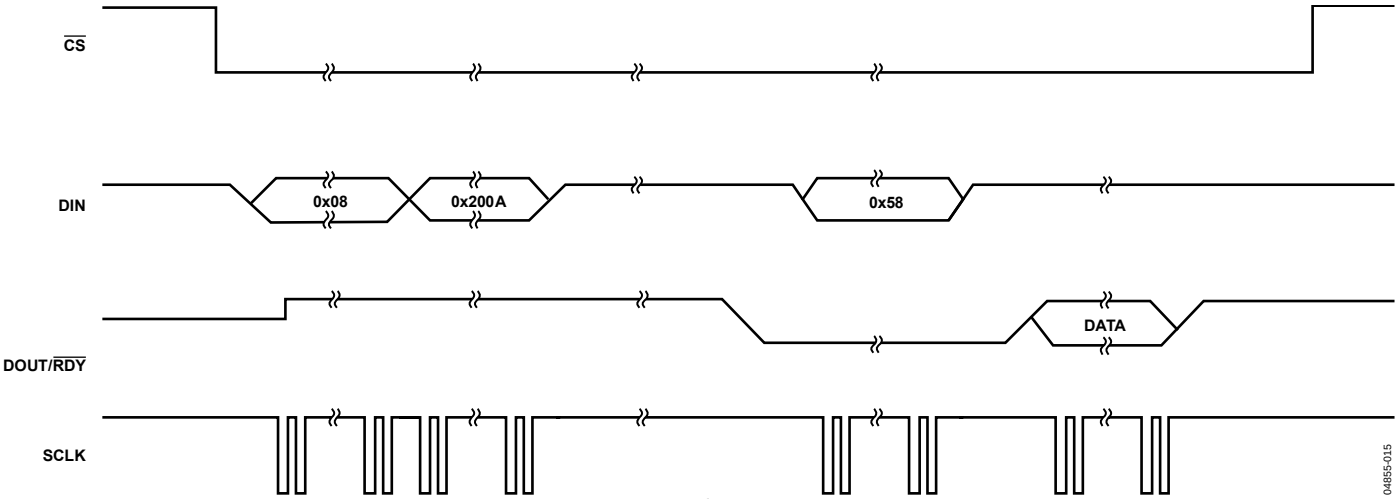


Figure 17. Single Conversion

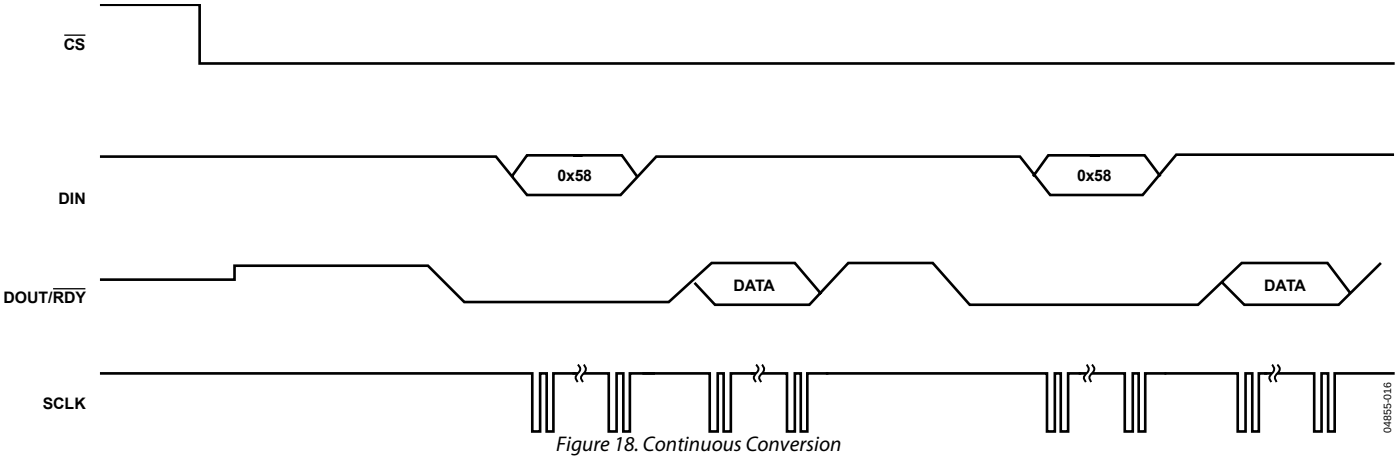


Figure 18. Continuous Conversion

Continuous Read

Rather than write to the communications register each time a conversion is complete to access the data, the AD7792/AD7793 can be configured so that the conversions are placed on the DOUT/$\overline{\text{RDY}}$ line automatically. By writing 01011100 to the communications register, the user needs only to apply the appropriate number of SCLK cycles to the ADC, and the 16/24-bit word is automatically placed on the DOUT/$\overline{\text{RDY}}$ line when a conversion is complete. The ADC should be configured for continuous conversion mode.

When DOUT/$\overline{\text{RDY}}$ goes low to indicate the end of a conversion, sufficient SCLK cycles must be applied to the ADC, and the data conversion is placed on the DOUT/$\overline{\text{RDY}}$ line. When the conversion is read, DOUT/$\overline{\text{RDY}}$ returns high until the next conversion is available. In this mode, the data can be read only once. In addition, the user must ensure that the data-word is read before the next conversion is complete. If the user has not read the conversion before the completion of the next conversion, or if insufficient serial clocks are applied to the AD7792/AD7793 to read the word, the serial output register is reset when the next conversion is completed, and the new conversion is placed in the output serial register.

To exit the continuous read mode, the instruction 01011000 must be written to the communications register while the DOUT/$\overline{\text{RDY}}$ pin is low. While in the continuous read mode, the ADC monitors activity on the DIN line so that it can receive the instruction to exit the continuous read mode. Additionally, a reset occurs if 32 consecutive 1s are seen on DIN. Therefore, DIN should be held low in continuous read mode until an instruction is written to the device.

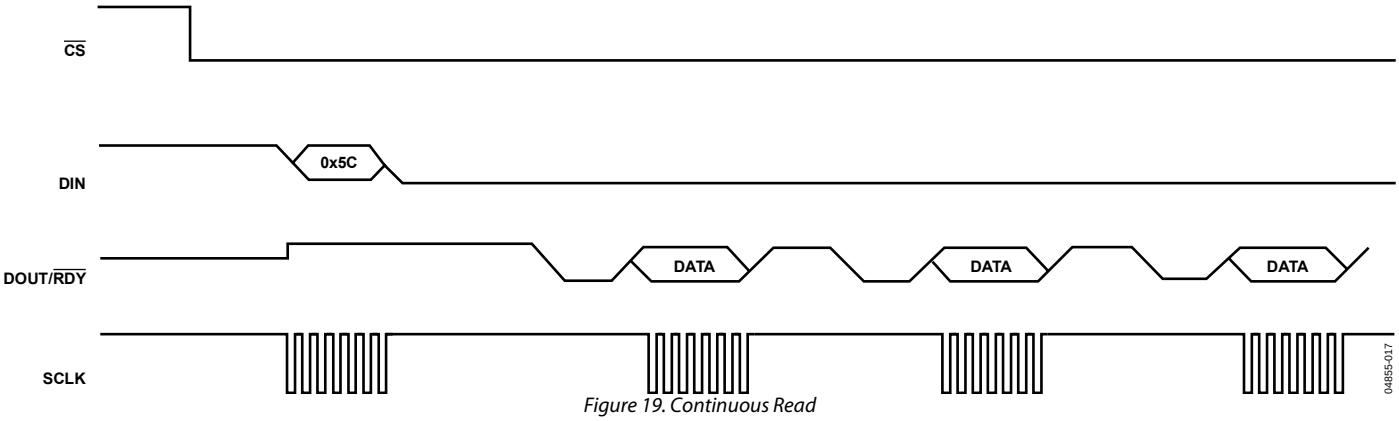


Figure 19. Continuous Read

CIRCUIT DESCRIPTION

ANALOG INPUT CHANNEL

The AD7792/AD7793 have three differential analog input channels. These are connected to the on-chip buffer amplifier when the device is operated in buffered mode and directly to the modulator when the device is operated in unbuffered mode. In buffered mode (the BUF bit in the mode register is set to 1), the input channel feeds into a high impedance input stage of the buffer amplifier. Therefore, the input can tolerate significant source impedances and is tailored for direct connection to external resistive-type sensors, such as strain gauges or resistance temperature detectors (RTDs).

When BUF = 0, the part is operated in unbuffered mode. This results in a higher analog input current. Note that this unbuffered input path provides a dynamic load to the driving source. Therefore, resistor/capacitor combinations on the input pins can cause gain errors, depending on the output impedance of the source that is driving the ADC input. Table 19 shows the allowable external resistance/capacitance values for unbuffered mode such that no gain error at the 20-bit level is introduced.

Table 19. External R-C Combination for No 20-Bit Gain Error

C (pF)	R (Ω)
50	9 k
100	6 k
500	1.5 k
1000	900
5000	200

The AD7792/AD7793 can be operated in unbuffered mode only when the gain equals 1 or 2. At higher gains, the buffer is automatically enabled. The absolute input voltage range in buffered mode is restricted to a range between GND + 100 mV and AV_{DD} – 100 mV. When the gain is set to 4 or higher, the in-amp is enabled. The absolute input voltage range when the in-amp is active is restricted to a range between GND + 300 mV and AV_{DD} – 1.1 V. Take care in setting up the common-mode voltage so that these limits are not exceeded to avoid degradation in linearity and noise performance.

The absolute input voltage in unbuffered mode includes the range between GND – 30 mV and AV_{DD} + 30 mV as a result of being unbuffered. The negative absolute input voltage limit does allow the possibility of monitoring small true bipolar signals with respect to GND.

INSTRUMENTATION AMPLIFIER

Amplifying the analog input signal by a gain of 1 or 2 is performed digitally within the AD7792/AD7793. However, when the gain equals 4 or higher, the output from the buffer is applied to the input of the on-chip instrumentation amplifier. This low noise in-amp means that signals of small amplitude can be gained within the AD7792/AD7793 while still maintaining excellent noise performance.

For example, when the gain is set to 64, the rms noise is 40 nV typically, which is equivalent to 21 bits effective resolution or 18.5 bits peak-to-peak resolution.

The AD7792/AD7793 can be programmed to have a gain of 1, 2, 4, 8, 16, 32, 64, and 128 using Bit G2 to Bit G0 in the configuration register. Therefore, with an external 2.5 V reference, the unipolar ranges are from 0 mV to 20 mV to 0 V to 2.5 V while the bipolar ranges are from ±20 mV to ±2.5 V. When the in-amp is active (gain ≥ 4), the common-mode voltage (AIN(+) + AIN(–))/2 must be greater than or equal to 0.5 V.

If the AD7792/AD7793 are operated with an external reference that has a value equal to AV_{DD}, the analog input signal must be limited to 90% of V_{REF}/gain when the in-amp is active, for correct operation.

BIPOLAR/UNIPOLAR CONFIGURATION

The analog input to the AD7792/AD7793 can accept either unipolar or bipolar input voltage ranges. A bipolar input range does not imply that the part can tolerate negative voltages with respect to system GND. Unipolar and bipolar signals on the AIN(+) input are referenced to the voltage on the AIN(–) input. For example, if AIN(–) is 2.5 V, and the ADC is configured for unipolar mode and a gain of 1, the input voltage range on the AIN(+) pin is 2.5 V to 5 V.

If the ADC is configured for bipolar mode, the analog input range on the AIN(+) input is 0 V to 5 V. The bipolar/unipolar option is chosen by programming the U/$\overline{B}$ bit in the configuration register.

DATA OUTPUT CODING

When the ADC is configured for unipolar operation, the output code is natural (straight) binary with a zero differential input voltage resulting in a code of 00...00, a midscale voltage resulting in a code of 100...000, and a full-scale input voltage resulting in a code of 111...111. The output code for any analog input voltage can be represented as

$$Code = (2^N \times AIN \times GAIN)/V_{REF}$$

When the ADC is configured for bipolar operation, the output code is offset binary with a negative full-scale voltage resulting in a code of 000...000, a zero differential input voltage resulting in a code of 100...000, and a positive full-scale input voltage resulting in a code of 111...111. The output code for any analog input voltage can be represented as

$$Code = 2^{N-1} \times [(AIN \times GAIN / V_{REF}) + 1]$$

where *AIN* is the analog input voltage, *GAIN* is the in-amp setting (1 to 128), and *N* = 16 for the AD7792 and *N* = 24 for the AD7793.

BURNOUT CURRENTS

The AD7792/AD7793 contain two 100 nA constant current generators, one sourcing current from AV_{DD} to AIN(+) and one sinking current from AIN(–) to GND. The currents are switched to the selected analog input pair. Both currents are either on or off, depending on the burnout current enable (BO) bit in the configuration register. These currents can be used to verify that an external transducer is still operational before attempting to take measurements on that channel. Once the burnout currents are turned on, they flow in the external transducer circuit, and a measurement of the input voltage on the analog input channel can be taken. If the resultant voltage measured is full scale, the user needs to verify why this is the case. A full-scale reading could mean that the front-end sensor is open circuit. It could also mean that the front-end sensor is overloaded and is justified in outputting full scale, or the reference may be absent, thus clamping the data to all 1s.

When reading all 1s from the output, the user needs to check these three cases before making a judgment. If the voltage measured is 0 V, it may indicate that the transducer has short circuited. For normal operation, these burnout currents are turned off by writing a 0 to the BO bit in the configuration register. The current sources work over the normal absolute input voltage range specifications with buffers on.

EXCITATION CURRENTS

The AD7792/AD7793 also contain two matched, software configurable, constant current sources that can be programmed to equal 10 μA, 210 μA, or 1 mA. Both source currents from the AV_{DD} are directed to either the IOUT1 or IOUT2 pin of the device. These current sources are controlled via bits in the IO register. The configuration bits enable the current sources, direct the current sources to IOUT1 or IOUT2, and select the value of the current. These current sources can be used to excite external resistive bridge or RTD sensors.

BIAS VOLTAGE GENERATOR

A bias voltage generator is included on the AD7792/AD7793. This biases the negative terminal of the selected input channel to $AV_{DD}/2$. It is useful in thermocouple applications, because the voltage generated by the thermocouple must be biased about some dc voltage if the gain is greater than 2. This is necessary because the instrumentation amplifier requires headroom to ensure that signals close to GND or AV_{DD} are converted accurately.

The bias voltage generator is controlled using the VBIAS1 and VBIAS0 bits in conjunction with the boost bit in the configuration register. The power-up time of the bias voltage generator is dependent on the load capacitance. To accommodate higher load capacitances, the AD7792/AD7793 have a boost bit. When this bit is set to 1, the current consumed by the bias voltage generator increases, so that the power-up time is considerably reduced. Figure 10 shows the power-up time when boost equals 0 and 1 for different load capacitances.

The current consumption of the AD7792/AD7793 increases by 40 μA when the bias voltage generator is enabled, and boost equals 0. With the boost function enabled, the current consumption increases by 250 μA.

REFERENCE

The AD7792/AD7793 have an embedded 1.17 V reference that can be used to supply the ADC, or an external reference can be applied. The embedded reference is a low noise, low drift reference, the drift being 4 ppm/°C typically. For external references, the ADC has a fully differential input capability for the channel. The reference source for the AD7792/AD7793 is selected using the REFSEL bit in the configuration register. When the internal reference is selected, it is internally connected to the modulator. It is not available on the REFIN pins.

The common-mode range for these differential inputs is from GND to AV_{DD}. The reference input is unbuffered; therefore, excessive R-C source impedances introduce gain errors. The reference voltage REFIN (REFIN(+) − REFIN(−)) is 2.5 V nominal, but the AD7792/AD7793 are functional with reference voltages from 0.1 V to AV_{DD}. In applications where the excitation (voltage or current) for the transducer on the analog input also drives the reference voltage for the part, the effect of the low frequency noise in the excitation source is removed because the application is ratiometric. If the AD7792/AD7793 are used in a nonratiometric application, a low noise reference should be used.

Recommended 2.5 V reference voltage sources for the AD7792/AD7793 include the ADR381 and ADR391, which are low noise, low power references. Also note that the reference inputs provide a high impedance, dynamic load. Because the input impedance of each reference input is dynamic, resistor/capacitor combinations on these inputs can cause dc gain errors, depending on the output impedance of the source that is driving the reference inputs.

Reference voltage sources like those recommended above (such as ADR391) typically have low output impedances and are, therefore, tolerant to having decoupling capacitors on REFIN(+) without introducing gain errors in the system. Deriving the reference input voltage across an external resistor means that the reference input sees a significant external source impedance. External decoupling on the REFIN pins is not recommended in this type of circuit configuration.

RESET

The circuitry and serial interface of the AD7792/AD7793 can be reset by writing 32 consecutive 1s to the device. This resets the logic, the digital filter, and the analog modulator while all on-chip registers are reset to their default values. A reset is automatically performed on power-up. When a reset is initiated, the user must allow a period of 500 μs before accessing any of the on-chip registers. A reset is useful if the serial interface becomes asynchronous due to noise on the SCLK line.

AV_{DD} MONITOR

Along with converting external voltages, the ADC can be used to monitor the voltage on the AV_{DD} pin. When Bit CH2 to Bit CH0 equal 1, the voltage on the AV_{DD} pin is internally attenuated by 6, and the resultant voltage is applied to the Σ-Δ modulator using an internal 1.17 V reference for analog-to-digital conversion. This is useful, because variations in the power supply voltage can be monitored.

CALIBRATION

The AD7792/AD7793 provide four calibration modes that can be programmed via the mode bits in the mode register. These are internal zero-scale calibration, internal full-scale calibration, system zero-scale calibration, and system full-scale calibration, which effectively reduces the offset error and full-scale error to the order of the noise. After each conversion, the ADC conversion result is scaled using the ADC calibration registers before being written to the data register. The offset calibration coefficient is subtracted from the result prior to multiplication by the full-scale coefficient.

To start a calibration, write the relevant value to the MD2 to MD0 bits in the mode register. After the calibration is complete, the contents of the corresponding calibration registers are updated, the $\overline{RDY}$ bit in the status register is set, the DOUT/$\overline{RDY}$ pin goes low (if $\overline{CS}$ is low), and the AD7792/AD7793 revert to idle mode.

During an internal zero-scale or full-scale calibration, the respective zero input and full-scale input are automatically connected internally to the ADC input pins. A system calibration, however, expects the system zero-scale and system full-scale voltages to be applied to the ADC pins before the calibration mode is initiated. In this way, external ADC errors are removed.

From an operational point of view, a calibration should be treated like another ADC conversion. A zero-scale calibration (if required) should always be performed before a full-scale calibration. System software should monitor the $\overline{RDY}$ bit in the status register or the DOUT/$\overline{RDY}$ pin to determine the end of calibration via a polling sequence or an interrupt-driven routine.

Both an internal offset calibration and a system offset calibration take two conversion cycles. An internal offset calibration is not needed, as the ADC itself removes the offset continuously.

To perform an internal full-scale calibration, a full-scale input voltage is automatically connected to the selected analog input for this calibration. When the gain equals 1, a calibration takes 2 conversion cycles to complete. For higher gains, 4 conversion cycles are required to perform the full-scale calibration. DOUT/$\overline{RDY}$ goes high when the calibration is initiated and returns low when the calibration is complete.

The ADC is placed in idle mode following a calibration. The measured full-scale coefficient is placed in the full-scale register of the selected channel. Internal full-scale calibrations cannot be performed when the gain equals 128. With this gain setting, a system full-scale calibration can be performed. A full-scale calibration is required each time the gain of a channel is changed to minimize the full-scale error.

An internal full-scale calibration can be performed at specified update rates only. For gains of 1, 2, and 4, an internal full-scale calibration can be performed at any update rate. However, for higher gains, internal full-scale calibrations can be performed when the update rate is less than or equal to 16.7 Hz, 33.2 Hz, and 50 Hz only. However, the full-scale error does not vary with update rate, so a calibration at one update rate is valid for all update rates (assuming the gain or reference source is not changed).

A system full-scale calibration takes 2 conversion cycles to complete, irrespective of the gain setting. A system full-scale calibration can be performed at all gains and all update rates. If system offset calibrations are being performed along with system full-scale calibrations, the offset calibration should be performed before the system full-scale calibration is initiated.

GROUNDING AND LAYOUT

Because the analog inputs and reference inputs of the ADC are differential, most of the voltages in the analog modulator are common-mode voltages. The excellent common-mode rejection of the part removes common-mode noise on these inputs. The digital filter provides rejection of broadband noise on the power supply, except at integer multiples of the modulator sampling frequency. The digital filter also removes noise from the analog and reference inputs, provided that these noise sources do not saturate the analog modulator. As a result, the AD7792/AD7793 are more immune to noise interference than a conventional high resolution converter. However, because the resolution of the AD7792/AD7793 is so high, and the noise levels from the AD7792/AD7793 are so low, care must be taken with regard to grounding and layout.

The printed circuit board that houses the AD7792/AD7793 should be designed such that the analog and digital sections are separated and confined to certain areas of the board. A minimum etch technique is generally best for ground planes because it provides the best shielding.

It is recommended that the GND pins of the AD7792/AD7793 be tied to the AGND plane of the system. In any layout, it is important to keep in mind the flow of currents in the system, ensuring that the return paths for all currents are as close as possible to the paths the currents took to reach their destinations. Avoid forcing digital currents to flow through the AGND sections of the layout.

The ground planes of the AD7792/AD7793 should be allowed to run under the AD7792/AD7793 to prevent noise coupling. The power supply lines to the AD7792/AD7793 should use as wide a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never be run near the analog inputs.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but it is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, and signals are placed on the solder side.

Good decoupling is important when using high resolution ADCs. AV_{DD} should be decoupled with 10 µF tantalum in parallel with 0.1 µF capacitors to GND. DV_{DD} should be decoupled with 10 µF tantalum in parallel with 0.1 µF capacitors to the system's DGND plane, with the system's AGND to DGND connection being close to the AD7792/AD7793.

To achieve the best from these decoupling components, they should be placed as close as possible to the device, ideally right up against the device. All logic chips should be decoupled with 0.1 µF ceramic capacitors to DGND.

APPLICATIONS INFORMATION

The AD7792/AD7793 provide a low cost, high resolution analog-to-digital function. Because the analog-to-digital function is provided by a Σ-Δ architecture, the parts are more immune to noisy environments, making them ideal for use in sensor measurement and industrial and process control applications.

TEMPERATURE MEASUREMENT USING A THERMOCOUPLE

Figure 20 outlines a connection from a thermocouple to the AD7792/AD7793. In a thermocouple application, the voltage generated by the thermocouple is measured with respect to an absolute reference, so the internal reference is used for this conversion. The cold junction measurement uses a ratiometric configuration, so the reference is provided externally.

Because the signal from the thermocouple is small, the AD7792/AD7793 are operated with the in-amp enabled to amplify the signal from the thermocouple. As the input channel is buffered, large decoupling capacitors can be placed on the front end to eliminate any noise pickup that may be present in the thermocouple leads. The AD7792/AD7793 have a reduced common-mode range with the in-amp enabled, so the bias voltage generator provides a common-mode voltage so that the voltage generated by the thermocouple is biased up to $AV_{DD}/2$.

The cold junction compensation is performed using a thermistor in the diagram. The on-chip excitation current supplies the thermistor. In addition, the reference voltage for the cold junction measurement is derived from a precision resistor in series with the thermistor. This allows a ratiometric measurement so that variation of the excitation current has no effect on the measurement (it is the ratio of the precision reference resistance to the thermistor resistance that is measured).

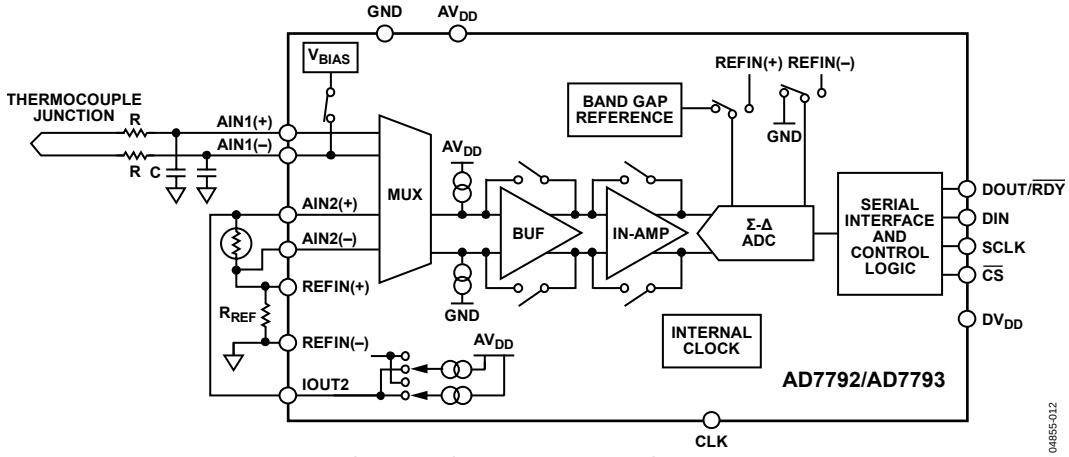


Figure 20. Thermocouple Measurement Using the AD7792/AD7793

TEMPERATURE MEASUREMENT USING AN RTD

To optimize a 3-wire RTD configuration, two identically matched current sources are required. The AD7792/AD7793, which contain two well-matched current sources, are ideally suited to these applications. One possible 3-wire configuration is shown in Figure 21. In this 3-wire configuration, the lead resistances result in errors if only one current is used, as the excitation current flows through RL1, developing a voltage error between AIN1(+) and AIN1(–). In the scheme outlined, the second RTD current source is used to compensate for the error introduced by the excitation current flowing through RL1. The second RTD current flows through RL2. Assuming RL1 and RL2 are equal (the leads would normally be of the same material and of equal length), and IOUT1 and IOUT2 match, the error voltage across RL2 equals the error voltage across RL1, and no error voltage is developed between AIN1(+) and AIN1(–). Twice the voltage is developed across RL3 but, because this is a common-mode voltage, it does not introduce errors. The reference voltage for the AD7792/AD7793 is also generated using one of these matched current sources. It is developed using a precision resistor and applied to the differential reference pins of the ADC. This scheme ensures that the analog input voltage span remains ratiometric to the reference voltage. Any errors in the analog input voltage due to the temperature drift of the excitation current are compensated by the variation of the reference voltage.

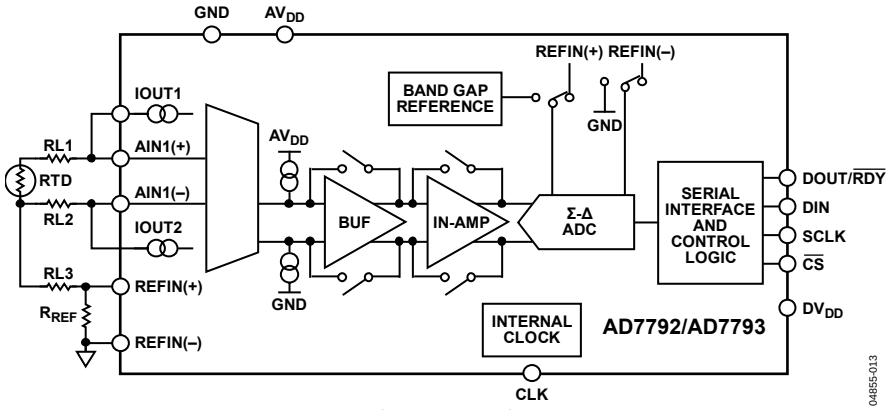


Figure 21. RTD Application Using the AD7792/AD7793

OUTLINE DIMENSIONS

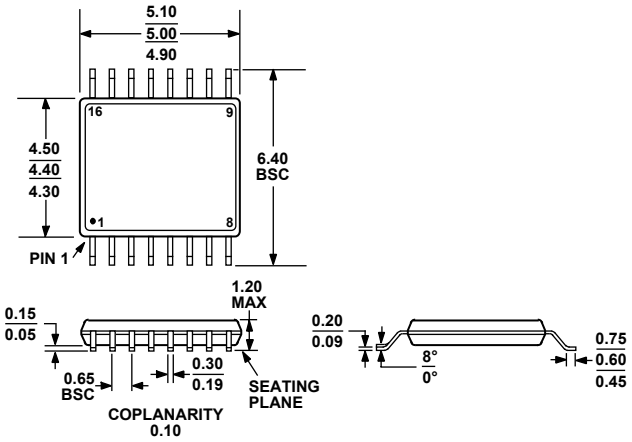


Figure 22. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7792BRU	–40°C to +105°C	16-Lead TSSOP	RU-16
AD7792BRU-REEL	–40°C to +105°C	16-Lead TSSOP	RU-16
AD7792BRUZ[1]	–40°C to +105°C	16-Lead TSSOP	RU-16
AD7792BRUZ-REEL[1]	–40°C to +105°C	16-Lead TSSOP	RU-16
AD7793BRU	–40°C to +105°C	16-Lead TSSOP	RU-16
AD7793BRU-REEL	–40°C to +105°C	16-Lead TSSOP	RU-16
AD7793BRUZ[1]	–40°C to +105°C	16-Lead TSSOP	RU-16
AD7793BRUZ-REEL[1]	–40°C to +105°C	16-Lead TSSOP	RU-16
EVAL-AD7792EBZ[1]		Evaluation Board	
EVAL-AD7793EBZ[1]		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

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